A STUDY OF
P-TYPE ACTIVATION
IN SILICON CARBIDE

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To my parents

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ABSTRACT

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Currently ion implantation is the main technique used to selectively dope regions in Silicon Carbide (SiC), but this method creates significant damage in the implanted regions. The implantation damage results in low doping activation and surface damage. The low activation along with the surface damage, which greatly affects surface mobility, is a major setback in device fabrication. To overcome the implantation damage, attempts at annealing at high temperatures have been made. The objective of this research is to study the activation of p-type Boron ion implantations in both 6H and 4H-SiC. The effect on the activation for different parameters, such as implant anneal temperature, implant dose, and polytype, were analyzed and compared. The activations obtained for the implant dose of 2.65E14 cm^{-2} in 6H-SiC at anneal temperatures of 1500°C, 1600°C, and 1700°C were 15-19.3%, 21.3-28.3%, and 30-36%, respectively. For implant dose of 1.3E15 cm^{-2} in 6H-SiC the activations at anneal temperatures of 1500°C, 1600°C, and 1700°C were 9.3-14.7%, 11.3-16%, and 15.3-36%, respectively. Lastly for implant dose of 1.3E15 cm^{-2} in 6H-SiC the activations at anneal temperatures of 1500°C, 1600°C, and 1700°C were 12-14.7%, 17.3-25.3%, and 22.7-44%, respectively. It was observed that higher implant anneal temperatures enhanced the percentage activated, higher implant doses reduced the activation percentage, the 4H polytype had a slightly improved activation ratio than 6H, and activation augmented with depth.

CHAPTER 1

INTRODUCTION

1.1 Properties of Silicon Carbide

Interest in Silicon Carbide (SiC) has grown because it has been recognized as having a great potential for applications involving high power, high temperature, and high frequency. It makes an attractive material for these applications because of it's wide bandgap which results in high thermal conductivity, high saturation drift velocity, lower thermal generation and a high breakdown field. Another benefit is its good physical and chemical stability and it is believed that the long-term reliability of SiC at elevated temperatures is much higher than other materials [1,2].

Though there are other wide gap materials with similar properties, SiC has some advantages, namely the more advanced substrate and epilayer growth technology, the availability of a semi-insulating epilayer, and the high quality thermally grown oxide [3]. But it also has some disadvantages such as a relatively low electron and hole mobility at room temperature as shown in Table 1.1 [1]. Another disadvantage is the negligible diffusion coefficients which makes the process of doping via diffusion impractical. Therefore other techniques have been investigated in the doping of SiC.

1.2 Doping Techniques - Ion Implantation vs. Diffusion

Doping plays an important role in the process of device fabrication. The different

Table 1.1

Comparison of Semiconductors [1].

Property	Si	GaAs	GaP	3C-SiC	Diamond
Bandgap (eV) at 300K	1.1	1.4	2.3	2.2 (2.9)	5.5
Maximum operating temperature (°C)	300	460	925	873 (1240)	1100(?)
Melting point (°C)	1420	1238	1470	Sublimes >1800	Phase change
Physical stability	Good	Fair	Fair	Excellent	Very good
Electron mobility R.T., (cm^2/V-s)	1400	8500	350	1000 (600)	2200
Hole mobility R.T., (cm^2/V-s)	600	400	100	40	1600
Breakdown voltage (V/cm)	0.3E6	0.4E6	-	4E6	10E6
Thermal conductivity (W/cm-°C)	1.5	0.5	0.8	5	20
Saturation electron drift velocity (cm/s)	1E7	2E7	-	2.5E7	2.7E7
Dielectric constant, K	11.8	12.8	11.1	9.7	5.5

ways of doping a material are doping during crystal growth, diffusion of dopants into the material, and ion implantation. Doping during crystal growth does not allow selective doping of different regions. Therefore for selective doping, diffusion or ion implantation is usually used. However diffusion in SiC is not feasible because of the extreme hardness and physical stability of the material which makes the diffusion coefficients negligible at temperatures below 1500°C [4]. Although, it is known that high temperatures of ~2000°C are required for dopant diffusion in SiC [5]. Therefore ion implantation appears as the only technique currently available for selective area doping.

A shortcoming of ion implantation has been the high density of crystal defects introduced due to the process of ions bombarding into the material during implantation. The implantation damage also results in low doping activation and surface damage. The low activation along with the surface damage, which greatly affects the surface mobility, is a major setback in device fabrication. To overcome the implantation damage, attempts at annealing at high temperatures have been made.

1.3 Implantation Annealing and its Relation to the Activation

During the implantation process, ion impact can dislodge atoms out of the SiC lattice, damaging the implanted region of the crystal. If the dose is high enough, the implanted layer can become amorphous. The ease of formation of an amorphous layer is dependent on the impurity and the substrate temperature. The heavier the impurity the lower the dose required to create an amorphous layer. At sufficiently high implant temperatures, an amorphous layer can no longer be formed.

Implantation damage can be removed by high temperature annealing. The high temperature causes the SiC atoms to move back to the lattice sites, and the impurity atoms enter substitutional sites in the lattice. This results in the implanted dose becoming electrically activated [6]. The dose electrically activated is highly dependent on the temperature and the duration of the anneal. The percentage of the dose that is electrical activated to the total dose can be determined from the capacitance vs. voltage

characteristic.

Annealing of n-type (N^+) ion implantations in 4H-SiC through recent efforts have resulted in reasonable sheet resistances (542Ω/❑) and electrical activations greater than 50% [7]. Studies done on the annealing of p-type (Al^+ and B^+) implantations in SiC have not resulted in such low sheet resistances and high electrical activations. Electrical activation of Al implantations have been shown to be better than B, resulting in comparatively lower sheet resistances [8]. The studies on p-type implant activation, especially activation of B^+-implantation into SiC, have been limited.

The objective of this paper is to investigate the electrical activation of boron ion-implantations into n-type 6H and 4H SiC epilayers. The electrical properties of the implanted layers after annealing at high-temperatures are analyzed. In this study the effect of impurity dose concentration, anneal temperature and time, and the SiC polytype on the electrical activation percentage is also investigated. Results from optical microscopy and capacitance-voltage measurements are discussed and compared to current publishings.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Silicon Carbide (SiC) exists in different crystal formations. These formations are known as polytypes. All polytypes are alike in two dimensional planes but differ in the stacking sequence in the dimension perpendicular to these planes. In SiC the stacking sequence of the close-packed planes of covalently bonded primary coordination tertrahedra can be described by the ABC notation. If the pure ABC stacking is repetitive, one obtains the zincblende structure. This is only the cubic SiC polytype and is referred to as 3C or β-SiC, where the 3 refers to the number of planes in the periodic sequence. The hexagonal (..ABAB..) sequence is also found in SiC. Furthermore, both can also occur in more complex, intermixed, forms yielding a wider range of ordered, large period, stacked hexagonal or rhombohedral structures of which 6H and 4H are the most common. All of these non-cubic structures are known as α-SiC [9,10]. These structures are shown in Fig. 2.1.

The properties of the different SiC polytypes differ, some of which are shown in Table 2.1. For power applications 4H might be preferred to 6H because of its higher mobility and theoretically higher breakdown electric field [11]. Both 6H and 4H are commercially available and show anisotropic behavior in contrast to 3C-SiC. In 4H-SiC the electronic mobility is about 1.2 times higher in the direction perpendicular to the (0001) plane to that in the parallel direction, however in 6H-SiC the electron mobility is

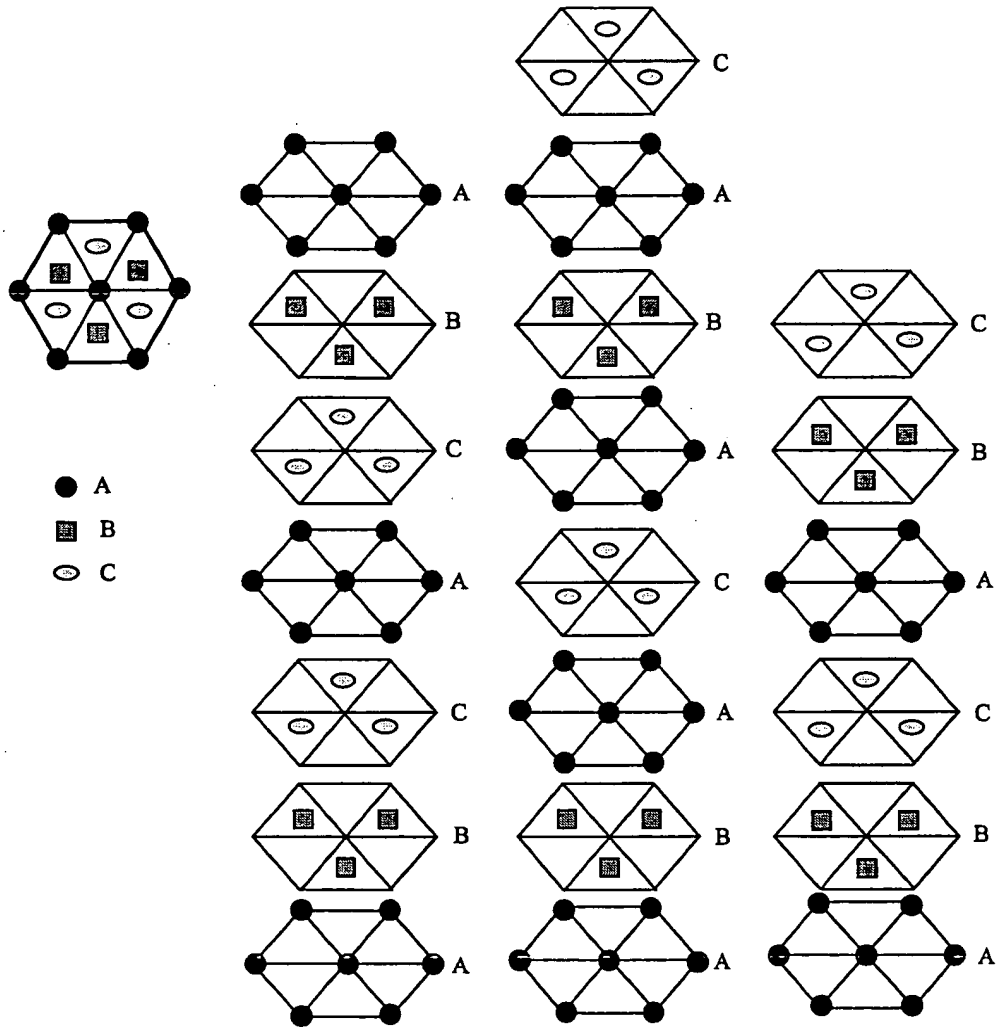


Fig. 2.1. Common SiC polytype structures [9].

Table 2.1

The properties of the different SiC polytypes [9].

	6H-SiC	4H-SiC	3C-SiC
Bandgap (eV)	2.9	3.3	2.2
Breakdown voltage (V/cm)	2.5E6	2.2E6	2E6
Electron mobility R.T., (cm^2/V-s)	400	800	1000
Hole mobility R.T., (cm^2/V-s)	50	70	40
Saturation electron drift velocity (cm/s)	2E7	2E7	2E7
Dielectric constant	9.8	9.8	9.8
Thermal conductivity (W/cm°C)	5	5	5

about 5 times lower to that in the parallel direction. Therefore, 4H-SiC is preferred for vertical devices while 6H-SiC is preferred for lateral devices [12].

Physical properties of a device also depend on the surface orientation. The metal Schottky barrier heights and oxidation rates are dependent on the crystal orientation. The (0001) directional plane produces the optimal metal-oxide-semiconductor interface quality [3]. The literature reviewed and the research work has been based on the (0001) direction surfaces.

2.2 Activation of P-type Ion Implantations in SiC

SiC can be doped either by in-situ doping or ion implantation. The disadvantage of in-situ doping during chemical vapor deposition (CVD) is that it does not allow for selective area doping because the impurities are introduced during the CVD process while the epilayer is grown, therefore the whole epilayer is doped. The doping efficiency is dependent on the type of face and the substrate temperature. It is much higher on a Si face than a C face and it decreases as the substrate temperature is increased. The lateral effect might be due to enhanced desorption of impurity atoms at high temperatures. Although n-type doping is easily achieved with low resistivity, p-type doping presents a problem as boron has a high ionization energy which makes it difficult to obtain low-resistivity (p^+) layers [8].

Due to the inadequacy of in-situ doping, the importance of ion-implantation has increased. The disadvantage with ion-implantation is the creation of lattice damage. To minimize this, proper implantation temperature and annealing processes are being researched. It has been reported that the use of elevated temperatures (800-1000°C) during implantation leads to strongly reduced crystalline defect densities. Subsequent heat treatments by rapid isothermal annealing (RIA) at 1060°C result in nearly perfect recrystallization of the implanted layers [4]. The crystal structure improvement results in an increase in the activation percentage.

For n-type doping, low sheet resistance of 542Ω/❑ for N^+ implantations in 4H-SiC at 500~800°C followed by a 1500°C anneal has been observed [8]. For p-type doping the best temperature and time for the highest activation is still an issue, as past implantation researches reported difficulties such as high sheet resistivity and low activation efficiency (<10%) [7]. It is known that high-temperature annealing of Al^+ and B^+ implantations is required to activate the implanted ions. Also, Al^+ implantation is more easily activated as compared to B to obtain a lower sheet resistance of 10~22kΩ/❑ [8].

Recent research has show that the activation ratio increases with an increase in temperature for both B and Al implantations in 4H-SiC [8]. Rutherford backscattering measurements showed that Al ions cause more severe damage in implanted layers than B ions, which could be attributed to the larger mass of Al ions. It was also found that complete amorphization for Al^+ and B^+ implantations occurred at the critical dose of 1E15 cm^{-2} and 5E15 cm^{-2}, respectively. When the dose did not exceed these critical values then the implanted layers could be activated by high temperature anneals [13]. The percentage activated was dependent on the temperature which is shown in Fig. 2.2. From the figure it can be seen that Al is more easily activated than B achieving a 100% activation at 1600°C as compared to 1700°C for B. The implantations were done at room temperature (RT) to obtain uniform box profiles with a total dose of 1E14 cm^{-2}. The implant dose and energies for Boron were 0.9E13 cm^{-2} at 30 keV, 1.1E13 cm^{-2} at 60 keV, 1.3E13 cm^{-2} at 100 keV, 1.8E13 cm^{-2} at 160 keV, 2.2E13 cm^{-2} at 250 keV, and 2.7E13 cm^{-2} at 360 keV. The anneal was performed in an Ar ambient for a duration of 30 min. The activation ratios were extracted from front to back Schottky C-V measurements done at a frequency of 100kHz. The lowest sheet resistance found for Al and B implants were 22kΩ/❑ at a dose of 2E15 cm^{-2} and 250kΩ/❑ [8].

Similar studies of boron implantations into n-type 4H-SiC [14] also indicated high activation ratios. However, the activation was obtained for a retrograde implant with doses and energies of 3.75E12 cm^{-2} at 30 keV, 5E12 cm^{-2} at 50 keV, 7.5E12 cm^{-2} at 100 keV, 2E13 cm^{-2} at 160 keV, 2.8E13 cm^{-2} at 240 keV, and 3.6E14 cm^{-2} at 320 keV. The

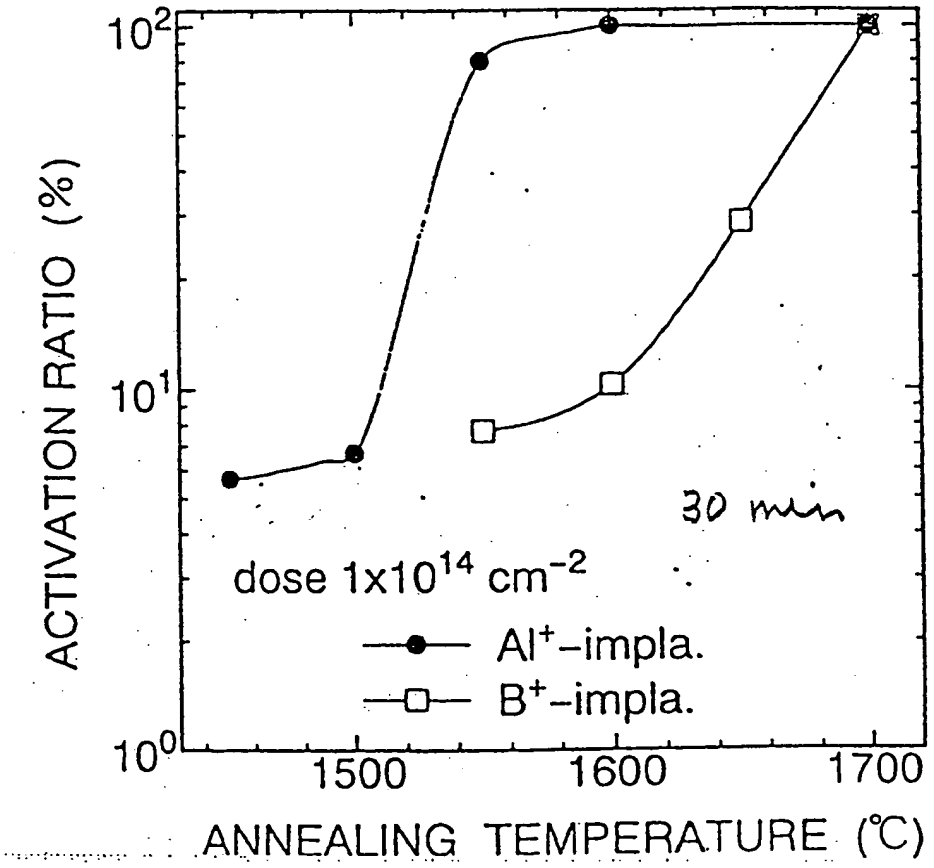


Fig. 2.2. Activation ratio vs. Annealing temperature for Al^+ and B^+ implantations in n-type 4H-SiC [8].

implantations were done at 600°C and annealed in an argon ambient for 40 min. The activation increased from 1% to a 100% with anneal temperatures of 1500°C to 1750°C, as seen in Fig. 2.3. Therefore the electrical activation of B implantation improves with an increase in anneal temperature.

Research on implantations of B into n-type 6H-SiC show that the degree of p-type activation after annealing at 1700°C to be in the range of 8 to 15% [15]. The implantation was performed at both room temperature and 500°C at subsequent energies from 30 to 300 keV and doses from 1E13 to 9E14 cm^{-2}. The anneal was performed in an ambient of SiH_4 for a duration of 30 min. It was suspected that the electrical activation degree was affected by the out-diffusion of B due to the high annealing temperature. Similar observations were reported by T. Troffer [16] for B^+-implanted on 4H-SiC.

A new approach to improve activation and reduce implant damage by co-implanting C ions along with the impurities is being investigated [7]. It has been observed that Al atoms are activated as acceptors only when sitting at Si sites. The introduction of C ions causes more Si vacancies to be formed and therefore more Al atoms occupy Si sites, thus enhancing the activation efficiency. However the advantage of this co-implantation is dependent on the Al concentration. Al was implanted into 6H-SiC, and while implanting, the ratio of N_C/N_{Al} was kept one. The sheet resistance obtained was 10-20 kΩ/❑ at N_{Al}~1E21cm^{-3}. The activation efficiency increased by a factor of 10 due to the increase in hole concentration, resulting in an activation efficiency of about 100%, assuming an Al acceptor level of 200 meV [7].

Similar effects of co-implantation were seen with B and Al in 4H-SiC [17]. An increase in activation efficiency was observed when the impurities were co-implanted with C and a decrease was observed when co-implanted with Si. It has been observed that B and Al form shallow acceptor levels in SiC when incorporated into the Si sublattice sites. The 4H-SiC samples were implanted with C or Si at room temperature (RT) or 800°C followed by an implantation of B or Al ions at RT. The C or Si were implanted to obtain similar profiles as the B and Al implants. The samples were then annealed at 1630 or 1700°C for 30 min. [17]. The results of C and Si co-implants indicates that the hole concentration increases with C-coimplantations and decreases with

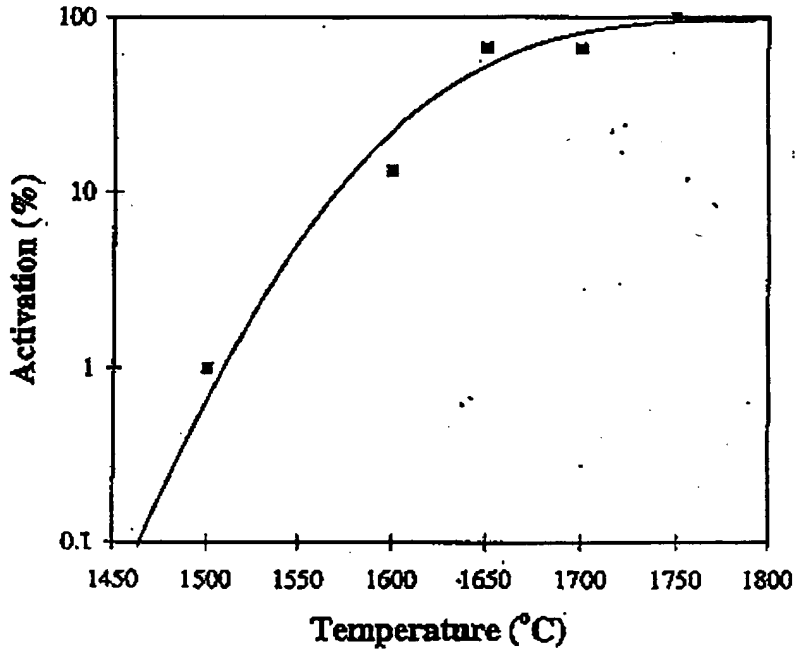


Fig. 2.3. Activation ratio vs. Annealing temperature for a retrograde B^+ implantation in n-type 4H-SiC [14].

Si-coimplantations. The increase and decrease in hole concentration decreases and increases the resistivity, respectively. Therefore C-coimplantations improve the electrical properties of p-type 4H-SiC. The implantations of C and Si increase the relative concentration of the interstitial C and Si atoms, respectively. These interstitials and the implanted B and Al atoms compete in recombining with Si and C vacancies during the annealing process and consequently influence the incorporation probability of B or Al at Si or C sublattice sites. In C-coimplantations an excess C interstitials occur which could reduce the C vacancies via recombination during annealing. This enhances the recombination of implanted B or Al with Si vacancies increasing their occurrence in the Si sublattice sites. In contrast the Si-coimplantation causes an excess of Si interstitials which reduces the Si vacancies resulting in a reduction of implanted B or Al occurrence in the Si sublattice sites. Therefore the shallow acceptor levels are increased by C-coimplantations and decreased by Si-coimplantation. The variation of the C concentration also affects the free hole concentration. It has been seen that the free hole concentration decreases with high C concentrations. This could be because the high concentration of C atoms gives rise to a high density of defects or carrier traps which result in the reduction of the free hole concentration. The effect of hot-coimplantatations was also conducted and it was observed that coimplantations at 800°C with C improved the free hole concentration.

The observation that B^+-implantations are more difficult to activate than Al^+-implantations in SiC may be due to a difference in the formations of defects. A desired outcome of the ion implantation is B atoms residing in Si lattice sites which causes the B to act as an acceptor. An undesired outcome is B-related defect centers called "D-centers". These D-centers are donor-like, which is presumed due to B atoms residing in C lattice sites and neighbouring intrinsic defect such as a Si vacancy. Therefore the formation of D-centers degrades the activation ratio after high-temperature implant anneals. It has been observed that coimplantation by C in B-implanted 6H-SiC decreases the donor-like D-center defects [18].

CHAPTER 3

CAPACITOR THEORY

3.1 Introduction

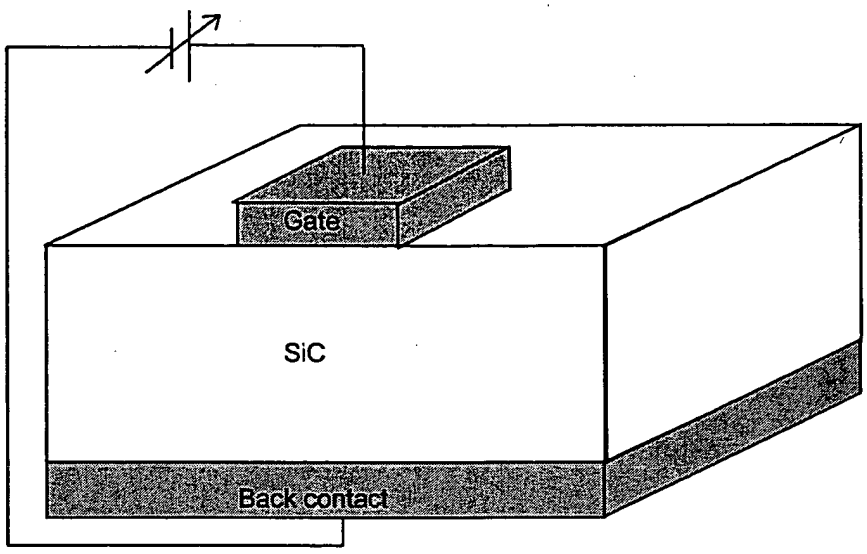
This chapter deals with the devices used to study the electrical activation obtained from the annealed p-type ion implanted regions. The activation is calculated from the doping that is extracted from the capacitance measurements. There are two capacitance measurement techniques used and compared, these are the MOS (Metal Oxide Semiconductor) capacitor and the Schottky capacitor. The ideal electrical behavior and non-ideal behavior are discussed in this chapter.

3.2 Schottky Capacitor

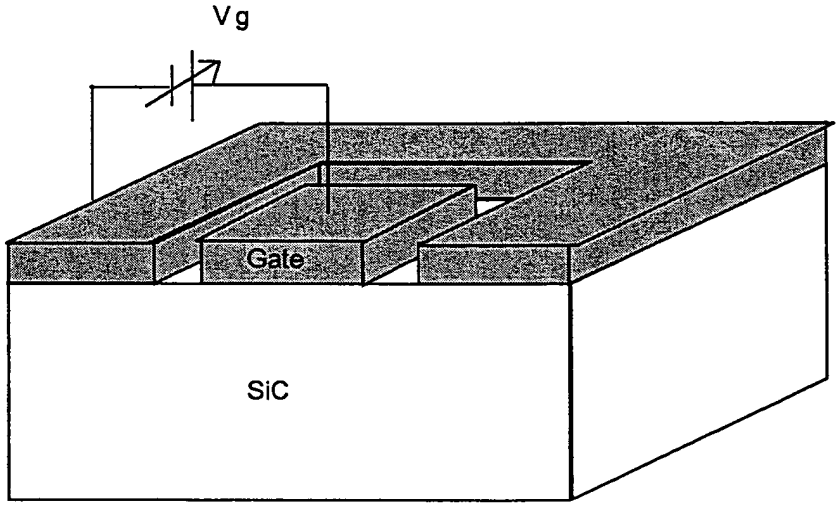
3.2.1 Structure

An ideal Schottky capacitor as shown in Fig. 3.1 (a) has no insulator between the metal and semiconductor. The front metal to semiconductor contact is Schottky while the back contact is ohmic.

A slightly modified Schottky capacitor structure shown in Fig. 3.1 (b) follows similar properties, but instead of a backside contact, a series Schottky contact is used.



(a)



(b)

Fig. 3.1. Schottky capacitor structures (a) Ideal structure (b) Modified structure used [19].

Since one of the capacitor contacts is much larger than the other, the capacitance nearly equivalent to a small area capacitor. The large contact is large enough to act as an AC short to the semiconductor, eliminating the need for a back contact. The advantage of this structure to the more common structure discussed previously is that the two gate metals can be fabricated simultaneously. Also it discards the problems of obtaining a good ohmic backside contact. An ohmic contact that is not good will have a low resistance that would result in erroneous capacitance values [19].

3.2.2 Capacitance-Voltage Characteristics

In the Schottky capacitor the measured capacitance varies as a function of the applied gate voltage. To measure these characteristics the device is positioned on a probing station, which is housed in a light-tight box, and connected by shield wires to a C-V bridge. The bridge superimposes a small ac signal on top of a preselected dc voltage and monitors the resulting ac current flow. A program is used to obtain a continuous capacitance versus voltage characteristic by slowly changing the dc voltage.

In an ideal Schottky model [20,21,22] the barrier height for the ideal metal-semiconductor Schottky contact, where the interface states are not considered, is equal to the difference between the work function of the metal Φm, which is dependent on the type of metal, and the electron affinity Xs, which is a property of the semiconductor. For a metal/p-type semiconductor the barrier height, ΦBp, can be expressed as

$$\Phi_{Bp} = E_g - (\Phi_m - X_s) \tag{3.1}$$

where Eg is the energy bandgap and q is the electronic charge. Φs is the semiconductor work function and is dependent of the doping type and concentration. For $\Phi m < \Phi s$ a potential barrier exists for holes to cross from the metal to the semiconductor and a nonlinear flow of current occurs, that is current flows easily in one direction but not the other, therefore a rectifying contact is formed. However, an ohmic contact is obtained if

$\Phi_m > \Phi_s$. The barrier height results in a potential difference, *Vbi*, shown in Fig. 3.2 (a), known as the contact potential expressed by

$$qV_{bi} = \Phi_m - \Phi_s = \Phi_{Bp} - (E_F - E_V) \tag{3.2}$$

where *EF* is the fermi level energy, and *EV* is the valence band energy.

For a p-type semiconductor when a negative voltage is applied to the Schottky contact, $V_A < 0$, the barrier height is reduced, shown in Fig. 3.2 (b), and current flows more easily resulting in the Schottky contact acting as a forward biased diode. When a positive voltage is applied, $V_A > 0$, the barrier height increases by $|qV_A|$, shown in Fig. 3.2 (c), and current flow is very small resulting in the Schottky contact acting as a reverse biased diode. *VA* also affects the depletion width. The small ac signal on top of a preselected dc voltage causes the charge increment at the depletion edge to change. Since this change in the depletion width is made by moving the majority carriers and the process is fast, the metal to depletion region to semiconductor can be represented as a parallel plate capacitor with the depletion region acting as an insulator. Therefore the depletion capacitance, *C(V)*, is

$$C(V) = \frac{A_G}{\sqrt{\frac{2(V_{bi} - V_A)}{qN_A K_s \varepsilon_0}}} \tag{3.3}$$

where *q* is the electronic charge, *AG* is the gate area, ε_0 is the permittivity of free space, *NA* is the acceptor doping concentration, and *Ks* is the dielectric constant of SiC. The depletion width, *W*, is dependent on the capacitance is

$$W = \frac{K_s \varepsilon_0 A_G}{C(V)} \tag{3.4}$$

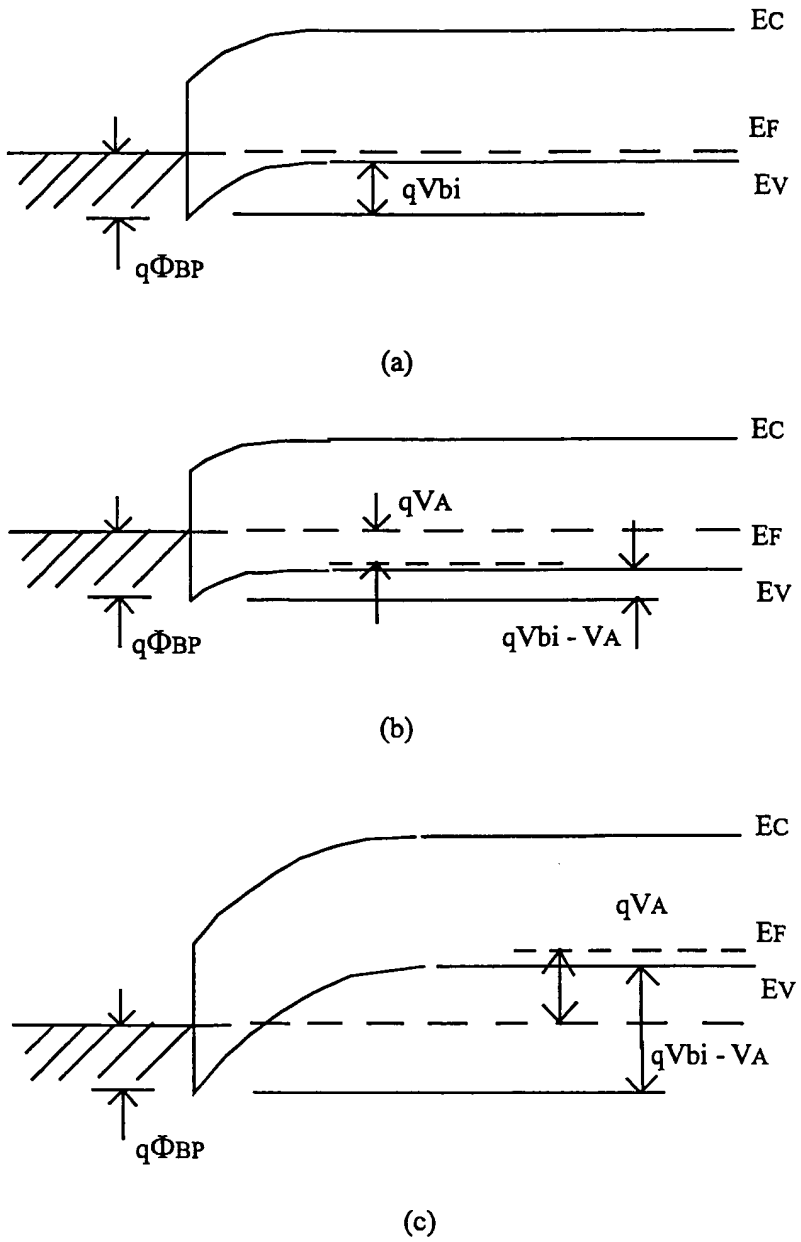


Fig. 3.2. Energy band diagrams for metal/p-type semiconductors when a (a) 0 bias voltage, (b) negative bias voltage, and (c) a positive bias voltage is applied [21].

3.2.3 Non-Idealities

There are some non-idealities with the Schottkty barrier [23,24,25], one of which is presence of interface states at the metal-SiC interface which is due to unsatisfied bonds or contamination on the SiC surface. These interface states charge and discharge as a function of bias, therefore affecting the charge distribution inside the device, and may

lead to a change in the barrier height, which affects the reverse saturation current, and hence cause a distorted or spread out nature of the the C-V characteristics.

A second deviation from ideal condition is the Schottky barrier lowering where Φ_{Bp} is not entirely independent of V_A [26]. This lowering results in a much larger reverse saturation current that increases with larger reverse bias. Therefore to minimize this, a metal with a large barrier height to SiC is used.

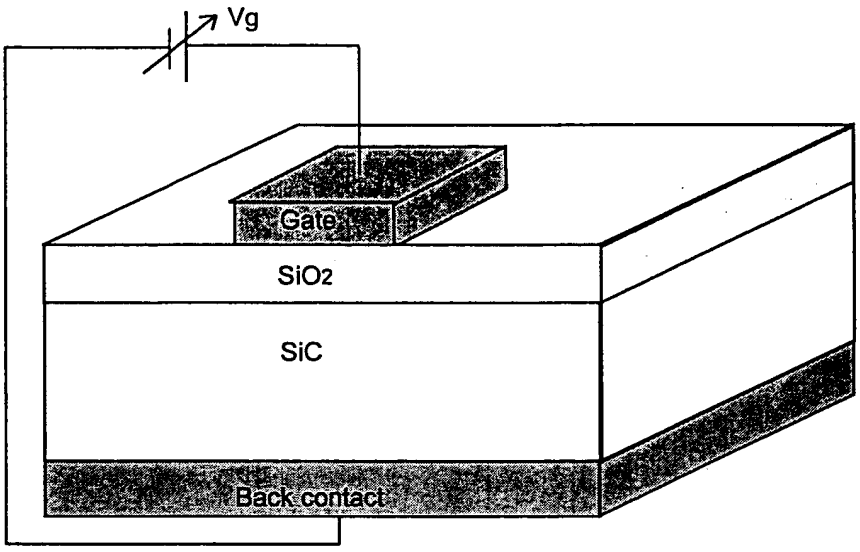
Another non-ideality is that the reverse saturation current in a Schottky barrier diode with large Φ_{Bp} is affected greatly by generation of holes and electrons in the depletion region. The generation current can increase the reverse current at room temperature. However, in SiC the generation process at room temperature is slow and this effect is negligible except very near breakdown.

The last deviation is the presence of series resistance associated with the bulk p-type semiconductor. In reverse bias conditions there is an additional AC voltage drop across the resistance, in series with the depletion capacitor, which also affects the C-V measurements.

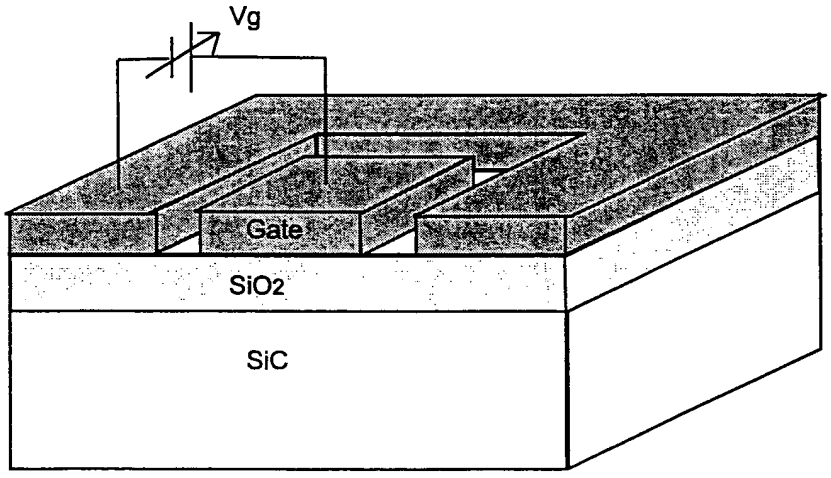
3.3 MOS Capacitor

3.3.1 Structure

An ideal MOS capacitor as shown in Fig. 3.3 (a) has the following properties: (i) the metallic gate is sufficiently thick to be considered an equipotential region under ac



(a)



(b)

Fig. 3.3. MOS capacitor structure (a) Ideal structure (b) Modified structure used [19].

and dc biasing conditions; (ii) the oxide is a perfect insulator with no current flow under all static biasing conditions; (iii) there are no charge centers located in the oxide or oxide-semiconductor interface; (iv) the backside contact is ohmic [27].

A slightly modified MOS capacitor structure shown in Fig. 3.3 (b) follows similar properties, but the difference is that instead of a backside contact a series MOS contact is used. Since one of the capacitor contacts is much larger than the other, the capacitance is nearly equivalent to a small area capacitor. The large contact acts as an AC short to the semiconductor, eliminating the need for a back contact. The advantage of this structure to the more common structure discussed previously is that the two gate metals can be fabricated simultaneously.

3.3.2 Capacitance-Voltage Characteristics

In the MOS capacitor the measured capacitance varies as a function of the applied gate voltage. To measure the characteristics, the device is positioned on a probing station, which is housed in a light-tight box, and connected by shield wires to a C-V bridge. The bridge superimposes a small ac signal on top of a preselected dc voltage and monitors the resulting ac current flow. The oxide acts as an insulator blocking the dc current flow. The ac signal is typically 15mV rms. A program is used to obtain a continuous capacitance versus voltage characteristic by slowly changing the dc voltage.

The C-V characteristic is formed from the response of the charge inside the p-type MOS-C to the applied ac signal as the dc bias is changed from accumulation, to depletion to inversion [28,29]. A negative voltage applied at the gate of the device results in majority carriers being attracted to the oxide-semiconductor interface, this is accumulation. When a small ac signal is applied the charge on the edges of the oxide is either added or subtracted, shown in Fig. 3.4 (a), which causes the charge configuration inside the accumulated MOS-C to act as a parallel plate capacitor for either high or low frequencies. Therefore the capacitance in accumulation is

$$C(acc) \approx C_{ox} = \frac{K_o \varepsilon_0 A_G}{x_o} \tag{3.5}$$

where xo is the oxide thickness, Cox is the oxide capacitance, and Ko is the oxide dielectric constant.

When a positive voltage is applied, the majority carriers withdraw from the oxide-semiconductor interface forming a depleted layer whose effective width is dependent on the applied depletion bias. Therefore the dc state is characterized by +Q charge on the gate and -Q depletion layer charge in the semiconductor, shown in Fig. 3.4 (b). When an ac signal is applied, the depletion width quasi-statically fluctuates about it's dc value. If the stationary dc charge is eliminated, then the small fluctuating charge on either side of the oxide at all probing frequencies is analogous to two parallel plate capacitors, Cox and Cs, in series where

$$C_{ox} = \frac{K_o \varepsilon_0 A_G}{x_o} \tag{3.6a}$$

$$C_s = \frac{K_s \varepsilon_0 A_G}{W(V)} \tag{3.6b}$$

and the capacitance in depletion, $C(depl)$, is expressed as

$$C(depl) = \frac{C_{ox} C_s}{C_{ox} + C_s} = \frac{C_{ox}}{1 + \frac{K_o W}{K_s x_o}} \tag{3.7}$$

When the bias is increased, an appreciable number of minority carriers can pile-up at the oxide-semiconductor interface and the dc width of the depletion layer tends to maximize at WT. In this inversion state the charge fluctuation depends on the frequency of the ac signal used in the C-V measurement. If the frequency is very low $(\omega \to 0)$, the minority

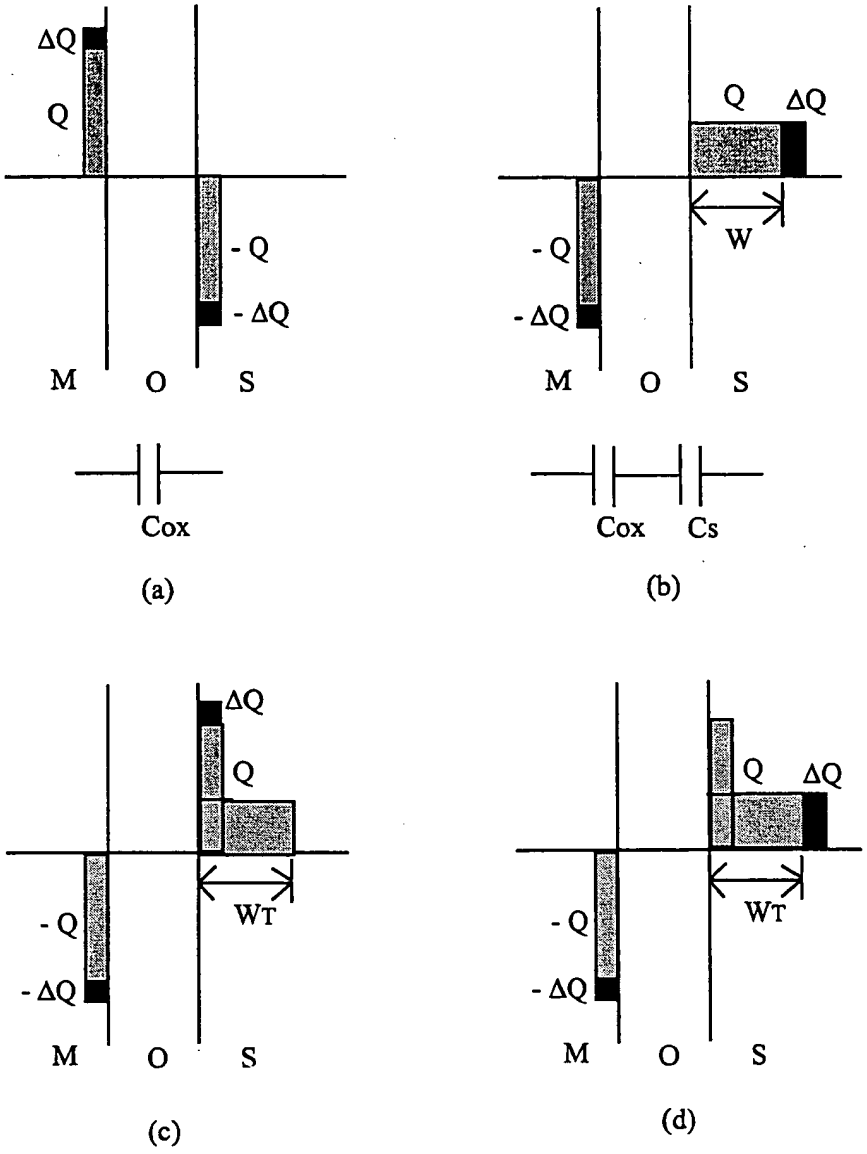


Fig. 3.4. AC charge fluctuations inside a p-type MOS-capacitor under dc biasing conditions corresponding to (a) accumulation, (b) depletion, (c) inversion when $(\omega \to 0)$, and (d) inversion when $(\omega \to \infty)$ [28].

carriers can be generated or annihilated in response to the applied ac signal. Therefore the capacitance in inversion, $C(inv)$, is expressed as

$$C(inv) \cong C_{ox} \tag{3.8}$$

At very high frequencies $(\omega \to \infty)$ the generation-recombination process is relatively slow which will eliminate the change in the minority carrier charge resulting in the depletion width fluctuating about the W_T dc value. This results in a similar behavior to the depletion bias region where the capacitance in inversion is represented as

$$C(inv) = \frac{C_{ox} C_s}{C_{ox} + C_s} = \frac{C_{ox}}{1 + \frac{K_o W_T}{K_s x_o}} \tag{3.9}$$

However in SiC at room temperatures the generation-recombination process is relatively slow even at low frequencies, therefore the capacitance in inversion can be represented as in (3.7) for low and high frequencies.

Since the depletion width changes with the applied gate bias, it is represented as

$$W(V) = \frac{K_s x_o}{K_o}\left[\sqrt{1 + \frac{V_G}{V_\delta}} - 1\right] \tag{3.10}$$

$$V_\delta = \frac{q K_s x_o^{\,2}}{2 K_o^{\,2} \varepsilon_0} N_A \tag{3.11}$$

The capacitance is represented as

$$C(V) = \frac{C_{ox}}{\sqrt{1 + \frac{V_G}{V_\delta}}} \tag{3.12}$$

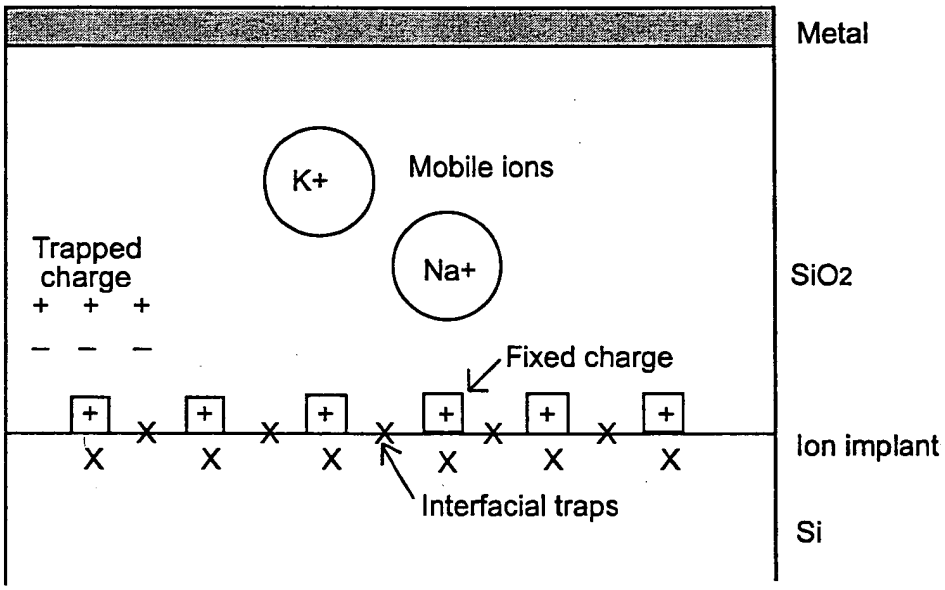


Fig. 3.5. Nature and location of charge centers in thermally grown SiO_2-SiC structures [31].

3.3.3 Non-Idealities

In ideal conditions flatband occurs at $V\delta = 0$, but since the vacuum levels in the metal and semiconductor are at different energies, ΦMS is not equal to 0, this results in a shift in the flatband voltage [30]. The difference in energies is called the built in potential, *Vbi*, and for p-type devices the flat-band voltage is laterally shifted ΦMS volts to the left.

Another nonideality is the presence of oxide charges such as mobile ions, fixed charge, and interfacial traps as shown in Fig. 3.5. These charges cause more significant effects, such as large voltage shifts and instabilities [31,32].

Mobile ions occur due to impurities in the oxide and cause voltage shifts. The positive ions give rise to a negative shift in the C-V characteristics and negative ions give rise to a positive shift. The voltage shift is also dependent on the position of the ions in the oxide, represented as

$$\Delta V_G(\text{mobile ions}) = -\frac{1}{K_o \varepsilon_0} \int_0^x x\, p_{ion}(x)\, dx \tag{3.13}$$

where $pion(x)$ is the concentration of ions at the depth of x. Under bias-temperature stressing the ions redistribute, affecting the voltage shift and resulting in inconsistency in the C-V measurements. Mobile ions are usually due to impurities during fabrication and are principally Na^+. To minimize the mobile ions in the oxide, contamination during fabrication can be minimized by cleaning the samples thoroughly and using reasonably clean oxidation furnaces.

Fixed charge, QF, is charge residing close to the oxide-semiconductor interface which stays fixed in position under bias-temperature stressing. These charges also cause a ΔVG shift.

$$\Delta V_G(\text{fixed charge}) = -\frac{Q_F}{C_{ox}} \tag{3.14}$$

Fixed charge is independent of the oxide thickness, semiconductor doping and semiconductor doping type. The fixed charge varies with the surface orientation and is also a strong function of the oxidation conditions such as the oxidizing ambient and furnace temperature. It decreases with increased oxidation temperatures. Annealing of an oxidized sample in an Ar or N_2 atmosphere for a sufficient time, to achieve steady state conditions, reduces the fixed oxide charge. This charge is due to excess ionic silicon that breaks away from the SiC and is waiting to react in the SiC-SiO_2 interface when the oxidation process is abruptly terminated. Therefore annealing in an inert atmosphere reduces the excess reaction components thereby lowering *QF*.

Interfacial traps cause a distorted or spread out nature of the C-V characteristics. They are allowed energy states in which electrons are localized in the vicinity of a material's surface and primarily arise from "dangling bonds" at the surface of the semiconductor. Like the fixed charge, the interfacial traps are dependent on the surface orientation. However the inert ambient anneal does not minimize the traps, but a re-oxidation anneal at 950°C for 3 hr. in wet O_2 does [33]. Therefore interfacial traps are minimized by a re-oxidation anneal.

$$\Delta V_G(\text{interfacialtraps}) = -\frac{Q_{IT}(\Phi_s)}{C_{ox}} \tag{3.15}$$

Hence the flat band voltage shift, *VFB*, is due to all these non-idealities and can be represented as

$$V_{FB} = \Phi_{MS} - \frac{1}{K_o \varepsilon_0} \int_0^x x\, p_{ion}(x)\, dx - \frac{Q_F}{C_{ox}} - \frac{Q_{IT}(\Phi_s)}{C_{ox}} \tag{3.16}$$

This affects the capacitance, resulting in

$$C(V) = \frac{C_{ox}}{\sqrt{1 + \frac{V_G - V_{FB}}{V_\delta}}} \tag{3.17}$$

It should be noted that in SiC, traps more than 0.5-0.6 eV above the valence band cannot fill fast enough to follow changes in the DC bias as the C-V curve is swept out, so these interface states do not affect the C-V curve at all.

3.4 Extraction of Doping and Activation Ratio from the C-V measurements

3.4.1 Schottky Capacitor

The doping in terms of the capacitance is obtained by manipulating (3.3) to get

$$N_A(W) = \frac{2}{qK_s \varepsilon_0 {A_G}^2 \, d\left(\left(\frac{1}{C(V)}\right)^2\right) \Big/ dV} \tag{3.18}$$

The depletion width in terms of the capacitance obtained from (3.4) is

$$W(V) = \frac{K_s \varepsilon_0 A_G}{C(V)} \tag{3.19}$$

3.4.2 MOS Capacitor

The doping in terms of the capacitance is obtained by substituting (3.11) into (3.12) to get

$$N_A(W) = \frac{2}{qK_s\varepsilon_0 A_G{}^2 \dfrac{d\left(\left(\dfrac{1}{C}-\dfrac{1}{C_{ox}}\right)^2\right)}{dV}} \tag{3.20}$$

The depletion in terms of the capacitance is obtained by substituting (3.12) into (3.10) to get

$$W(V) = K_s\varepsilon_0 A_G\left(\frac{1}{C(V)}-\frac{1}{C_{ox}}\right) \tag{3.21}$$

To obtain the flat band voltage, the bulk doping, *Nbulk*, from the average slope of $(1/C - 1/Cox)^2$ is calculated and plugged into the Debye length. In the bulk, or everywhere under flat band conditions, where the semiconductor can be viewed as having equal number of ionized impurity sites and mobile electrons and holes, the placement of charge near the semiconductor, for example on the MOS-C gate, causes the mobile species inside the semiconductor to rearrange so as to shield the semiconductor from the perturbing charge. The shielding distance or band bending region is on the order of the Debye length [34] which is

$$L_D = \sqrt{\frac{K_s\varepsilon_0 kT}{q^2 N_{bulk}}} \tag{3.22}$$

where k is the Boltzmann constant, and T is the temperature in Kelvin. Using this, the capacitance of the oxide in series with the flatband capacitance is obtained from the following equations

$$C_{sfb} = \frac{K_s \varepsilon_0 A_G}{L_D} \tag{3.23}$$

$$C_{fb} = \frac{C_{sfb} C_{ox}}{C_{sfb} + C_{ox}} \tag{3.24}$$

Using the value obtained for the flatband capacitance the flatband voltage can be obtained from the C-V data measured. The flatband voltage value is then be plugged into (3.17). The flat-band voltage indicates at what voltage the bulk starts to get depleted of majority carriers.

3.4.3 Activation Percentage

The activation ratio is the ratio of the dose that is electrically activated to the total dose implanted. This can be estimated from the ratio of the doping measured to the expected doping extracted from the simulated implant profiles.

$$Percent\ Activated = \frac{N_A}{N_{implanted}} 100 \tag{3.25}$$

This indicates the electrical activation of the implanted region.

CHAPTER 4

FABRICATION & MEASUREMENTS

4.1 Introduction

This chapter deals with the fabrication of Schottky capacitors and MOS capacitors in 6H and 4H SiC samples. The implantation, implant anneal, and oxidation conditions are presented. The measurement techniques used to obtain the C-V curves are also presented.

4.2 Fabrication

4.2.1 Wafer Specifications

The material used were from 13/8 inch diameter 6H and 4H SiC wafers produced by Cree Research Inc. Each wafer consisted of a substrate which was heavily doped in-situ during bulk growth with nitrogen for n-type. An epitaxial layer, also doped in-situ during growth with nitrogen, was grown on the Si-face (0001) of each wafer. Prior to epigrowth this face was polished. The epitaxial layer growth resulted in a Si-face, on which all processing was done. Table 4.1 displays the growth specifications for each wafer used.

Each wafer was sawed by Cree Research into 4 quarters. It was later diced, after

Table 4.1

SiC wafer specifications

Wafer number	G0590-11	H0612-3	Z0113-6
Wafer type	6H-SiC	6H-SiC	4H-SiC
Substrate doping type	N+	N+	N+
Substrate doping concentration (cm^{-3})	1.7E+18	1.5E+18	9.3E+18
Epi-layer doping type	N	N	N
Epi-layer doping concentration (cm^{-3})	5.1E+15	4.5E+15	4E+15
Epi-layer thickness (μm)	10	5	5

ion implantation, into smaller 1cm x 1cm pieces so that different experiments could be performed.

4.2.2 Ion Implantation

Prior to ion implantation, each new sample was cleaned, as specifed in the Appendix, to remove any contaminants and any native oxide from the surface. In order to minimize channeling effects an oxide layer was grown. A dry oxidation was done to grow a thin oxide layer of 20 nm using the Lindberg furnace lined with pure alumina. The oxidation was done in an oxygen ambient at 1200°C for 30 min. The samples were then sent for ion implantation.

The energies and doses for the implantation were determined by using an empirical implantation depth simulator from which the implant profile was simulated [35]. The implant profiles for each implant done is shown in Fig. 4.1. The first batch of samples were implanted twice with a total dose of 2.65E14 cm^{-2}. The first implant was done with dose and energies of 5.5E12 cm^{-2} at 20 keV, 1E13 cm^{-2} at 52 keV, 1.6E13 cm^{-2} at 110 keV, and 2.7E13 cm^{-2} at 200 keV. A second implant on the same sample was done with dose and energies of 9E12 cm^{-2} at 15 keV, 1.7E13 cm^{-2} at 40 keV, 3E13 cm^{-2} at 90 keV, 4E13 cm^{-2} at 170 keV, and 1.1E14 cm^{-2} at 300 keV. Both these implants resulted in the profile shown in Fig. 4.1 (a). A second batch of samples were implanted with a total dose of 1.3E15 cm^{-2}. The implant was done with dose and energies of 7E13 cm^{-2} at 15 keV, 1.4E14 cm^{-2} at 45 keV, 2.2E14 cm^{-2} at 100 keV, 3.2E14 cm^{-2} at 180 keV, and 5.6E14 cm^{-2} at 300 keV and resulted in the profile shown in Fig. 4.1 (b). Since a blanket implant was done an implant mask was not required. The ion implantations were all done at 650°C at an implant angle of 0° and a beam current of 50 mA. All ion implantations were done at Kroko Inc, Tustin, CA.

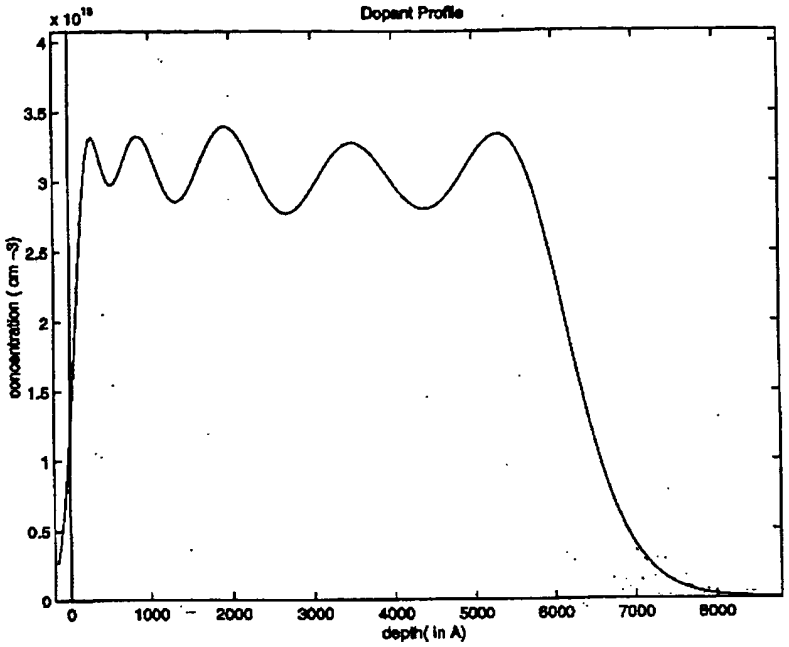
4.2.3 Implant Anneal

After the ion implantation was completed, the samples were diced into smaller

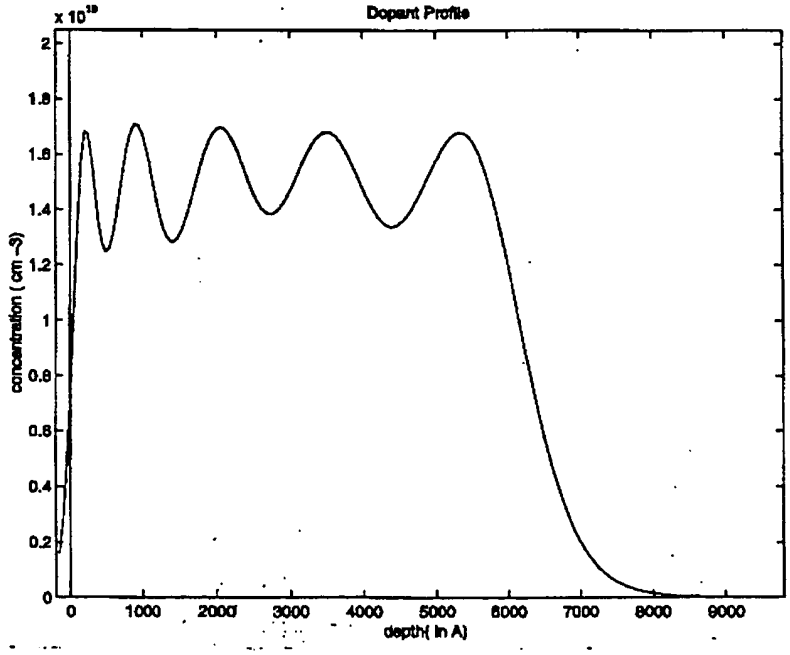
pieces so that different experiments could be done on the same implant profile. The samples then went through a post-implantation clean, stipulated in the Appendix. These samples were then sent to Air Force Research Lab/Materials Directorate for the implant anneals. All samples were annealed in a resistively-heated furnace with tungsten heating elements and tungsten and molybdenum heat shields. The furnace consisted of an enclosure of double-walled stainless steel for water cooling. The hot zone dimensions were: diameter: 3", height: 8". The maximum operating temperature was 2300°C and the ramp rates were as high as 4°C/sec. A mechanical roughing pump backed a turbomolecular pump. Vacuum in the mid 10^{-6} Torr range was achieved before backfilling with argon to pressures slightly above atmospheric pressure. A thermocouple was used to monitor temperature. The anneals were done at temperatures of 1500°C, 1600°C and 1700°C for a duration of 40 minutes each. All anneals were done without a SiC wafer cap.

4.2.4 Oxidation for MOS Devices

For the MOS devices an oxidation was done prior to metallization. Prior to the oxidation a thorough RCA clean, refer to the Appendix, was done to remove any contamination or metals from the surface. Thermal oxidation of SiC is similar to Si [36] as at high temperatures the oxygen combines with the Si bonds on the surface forming SiO_2. The succeeding oxidation occurs as O_2 or H_2O molecules diffuse through the existing SiO_2 layer to react with SiC at the SiC/SiO_2 interface. CO or CO_2 molecules formed by the reaction diffuses out through the SiO_2 and escapes as gas. This leads to the formation of an oxide layer. An oxide layer of about 40 nm was grown using the Blue-M furnace lined with quartz. The sample was oxidized in wet O_2 at 1130°C for 2.5 to 3 hrs. at atmospheric pressure and was followed by an in-situ argon anneal for 30 min. A wet oxidation was used to lessen interface states and an anneal in an inert ambient was used to diminish the fixed charge. The ramp rates of 15°C/min and 10°C/min to ramp up and ramp down the temperature, respectively, were used. The slow ramp rates were used to lessen the abruptness of the termination of the oxidation and thereby abate the formation



(a)



(b)

Fig. 4.1 Implant profiles (a) total dose 2.65E14 cm^{-2}, and (b) 1.3E15 cm^{-2}

of "dangling bonds" which would then reduce the interfacial trap charge.

4.2.5 Metallization

For the Schottky devices the samples are cleaned, refer to the Appendix, and any native oxide was removed after the implant anneal. The metal used was nickel (Ni) because it has a large barrier height to p-type SiC and makes good Schottky contacts. About 500 Angstroms of Ni was evaporated using the Varian E-beam evaporator. In the electron beam (E-beam) [37] evaporator a high-intensity beam of electrons is focused on a source target containing the metal to be evaporated. The energy from the electron beam melts a region of the target. Metal evaporates from the source and covers the SiC wafer with a thin layer. The wafers are mounted above the source, and the source material sits in a water-cooled crucible, and its surface only comes in contact with the electron beam during the evaporation process. Purity is controlled by the purity of the original source metal and by cleaning the samples prior to loading it into the evaporator. The supply of metal for evaporation is usually more than sufficient due to the relatively large size of the source. The deposition rate is controlled by changing the beam current and energy. The amount deposited is also monitored by a quartz crystal that gets covered by the evaporating metal during deposition. The resonant frequency of the crystal shifts in proportion to the thickness of the deposited film.

For the MOS devices the metal was evaporated onto the surface of the SiC wafer right after the oxidation was completed to improve the adhesiveness of the metal to the oxide. The metal used was aluminum (Al) because it makes a good contact to the oxide. About 2000-3000 Angstroms of aluminum was evaporated using the NRC evaporator. Similar to the E-beam evaporator, the metal was melted and evaporated onto the wafers, that were mounted above the source, covering the them with a thin layer. However instead of an electron beam the metal was melted by heating the tunsten boat, which contained the metal, by increasing the current through the boat. Purity was controlled by the purity of the original source metal and by cleaning the samples and utensils prior to loading it into the evaporator. The thickness of the metal evaporated was controlled by

the duration of evaporation and the deposition rate, which was dependent on the boat temperature.

4.2.5 Lithography

After the metal was evaporated onto the wafer, the sample went through a lithography step to pattern the devices [38]. Therefore, following metallization the wafers were cleaned and hardbaked to remove any moisture to ensure good photoresist adhesion. The photoresist is spun onto the wafer to obtain an even layer. The viscosity of the photoresist and the spin speed and spin time control the thickness of the photoresist. A positive photoresist, AZ1518, was used. A spin speed of 5000 RPM, and spin time of 40 sec. was used. The wafer was then softbaked at 85°C for 15 min. to improve adhesion and remove solvent from the photoresist. The wafer was then mounted on a mask aligner and the mask for patterning the devices, shown in Fig. 4.2, was aligned on top of the wafer. After that, the photoresist was exposed to ultraviolet (UV) light for 7.5 sec. The exposed resist was then washed away using a developer. For the Schottky devices with the nickel metal the developer used was a ratio of 1:5 of AZ 351developer to de-ionized (DI) water. For the MOS devices with the aluminum metal the developer used was a ratio of 1:1 of AZ developer to DI water. The different developers were used as the AZ 351 developer etched the aluminum, which made it difficult to determine when the develop was complete. After that, the wafer was hardbaked to harden the photoresist and improve the adhesion.

The next step was to etch the exposed metal. The etchant used for nickel consisted of a 1:4 ratio of nitric acid (HNO_3) and DI water. The etchant used for aluminum consisted of a 1:4:1:4 ratio of DI water, phosphoric acid (H_3PO_4), nitric acid (HNO_3) and acetic acid (CH_3COOH). The etch rate depended on the metal purity, existence of an oxidized layer on the surface, and the wafer temperature. After the etch was complete the photoresist was stripped and cleaned and the wafer was ready for measurements. Summary of the fabrication process is shown in the Appendix.

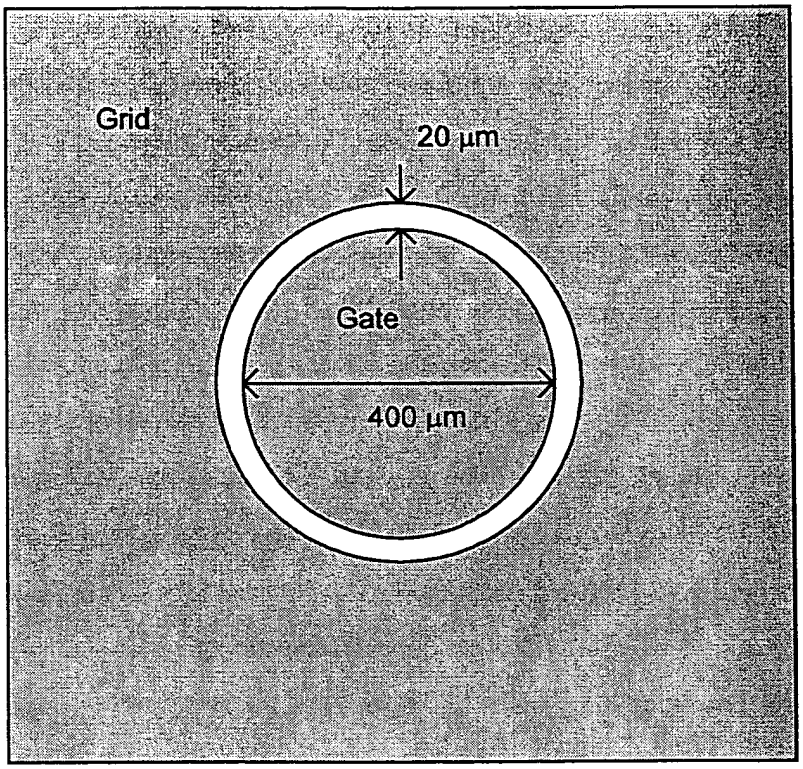


Fig. 4.2 Mask for MOS and Schottky contacts.

4.3 Measurement Techniques

For the Schottky capacitor the C-V characteristics of the device was measured by positioning the wafer on a probing station, which was housed in a light-tight box, and connected by shield wires to a C-V bridge. The bridge superimposed a small ac signal on a preselected dc voltage and monitored the resulting ac current flow. The HP 4274A multifrequency LCR meter was used to make the measurements. The CV.4274 program was used to obtain a continuous capacitance versus voltage characteristic by slowly changing the dc voltage. The C-V measurements were made at different frequencies and in the parallel and series mode.

Prior to making measurements, any stray capacitance between the probes or the probes and metal contact was removed by calibrating the C-V meter. The bias was turned off and a shielded wire was used to connect the two probe arms. The probes were brought into contact with the metal contact and raised slightly until no contact was made and the open circuit capacitance was calibrated. Using another shielded wire the two probes were shorted together and the short circuit capacitance was calibrated. This method eliminated the effect of any stray capacitance during measurements.

For the MOS capacitor the C-V characteristics of the device were measured by positioning the wafer on a probing station, which was housed in a light-tight box. Two techniques were used to make the measurements. In one the probes were connected by shield wires to a C-V bridge and the bridge superimposed a small ac signal on a preselected dc voltage and monitored the resulting ac current flow. In the other a Quasi-static CV meter was used, which measures the capacitance quasi-staticallyat an effective frequency of 0.25 Hz. The Keithley 595 Quasistatic CV meter controlled by the 590 CV Analyzer was used. The Keithley 5951 remote input coupler was used to connect the shielded wires to the CV meter. The Hilodas.bas program was used to obtain a continuous capacitance versus voltage characteristic by slowly changing the dc voltage. The measurements were made in the parallel mode. The measurement set-up for the Schottky and the MOS capacitor is shown in Fig. 4.3, and the Quasistatic MOS capacitor masurement setup is shown in Fig. 4.4.

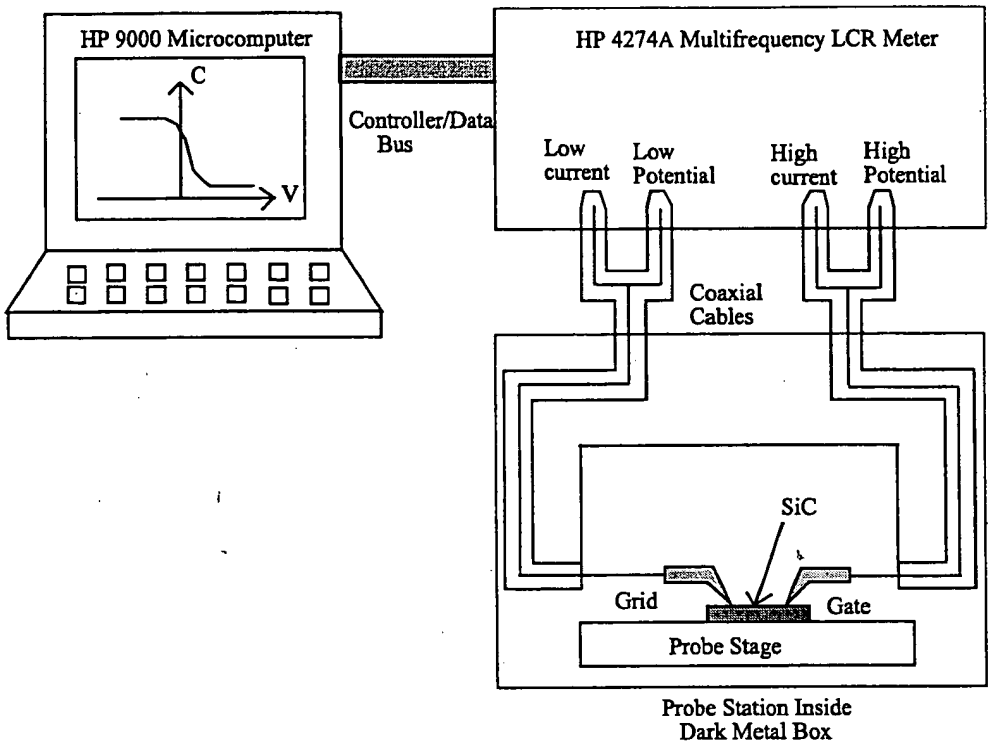


Fig. 4.3. C-V measurement setup for the Schottky and MOS capacitor measurements [19].

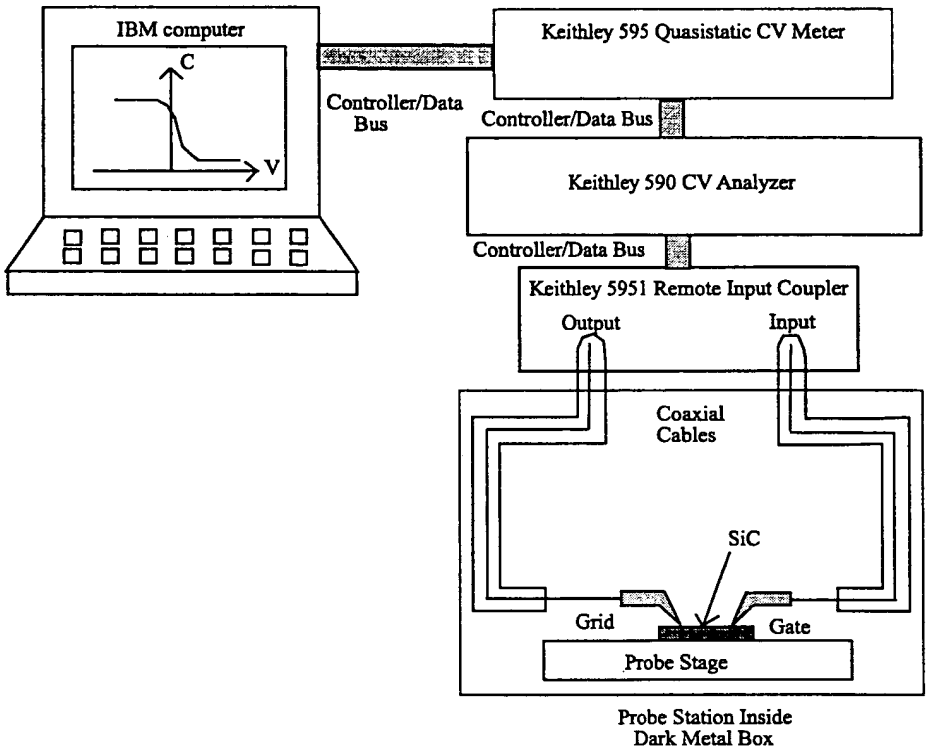


Fig. 4.4. C-V measurement setup for the Quasistatic MOS capacitor measurements.

The effect of any stray capacitance was eliminated by a technique similar to the Schottky measurement calibration technique. The probes were placed at close proximity to the metal contacts and the stray capacitance was calibrated to zero.

A measurement technique to observe the formation of an inversion layer was also used. Initially the bias was swept from accumulation to deep depletion in the dark. The device was then illumination by a tungsten lamp for about 3 min. after which it was turned off and the bias was swept back. When swept back the capacitance will increase if an inversion layer exists.

CHAPTER 5

EXPERIMENTAL RESULTS & DISCUSSION

5.1 Introduction

In this chapter the experimental data is presented and discussed. Both the Schottky and MOS C-V results are investigated and compared. The effect of sacrificial oxidation, series resistance, flatband voltage shift, and field inversion on the capacitance data is analyzed. The variations in the activation ratio between different annealing temperatures and implant dose are also investigated. These activation results are then compared to current findings.

5.2 Schottky Capacitor Measurements

5.2.1 Benefits of Sacrificial Oxidation

The effect of sacrificial oxidation on the capacitance-voltage (C-V) characteristics is considered. Sacrificial oxidation is the process where an oxide layer is grown and etched off. It's purpose is to remove any surface damage. The effect of sacrificial oxidation is illustrated in Fig. 5.1 and Fig. 5.2. It is seen that sacrificial oxidation significantly improves the C-V measurements and the surface.

Fig. 5.1 .C-V measurements were taken before and after the sacrificial oxidation.

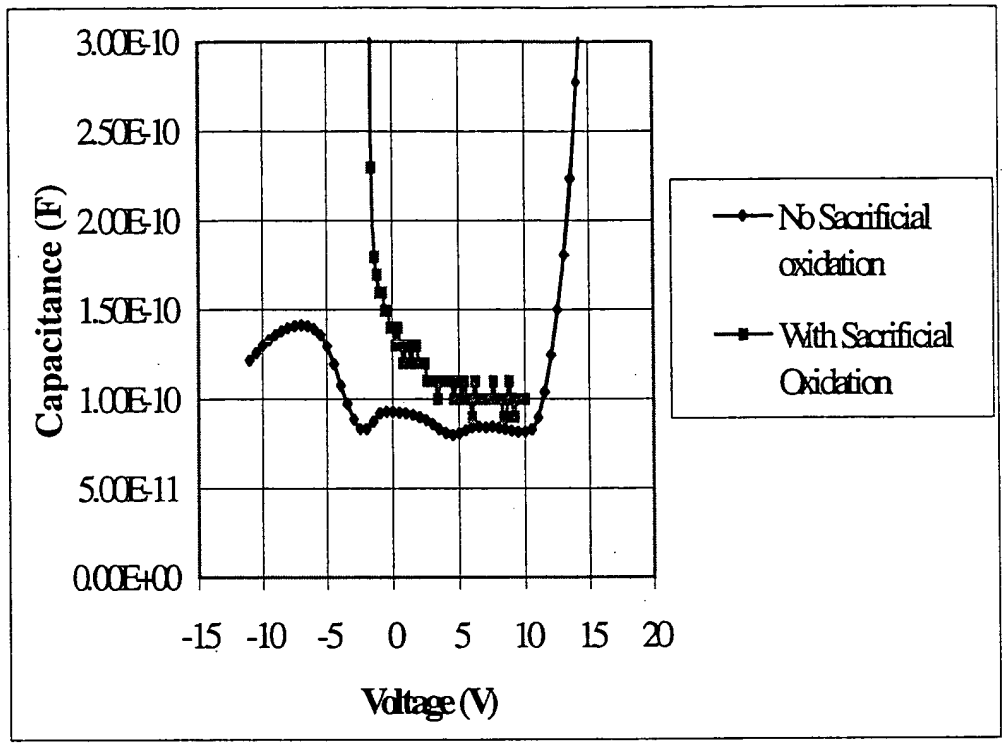
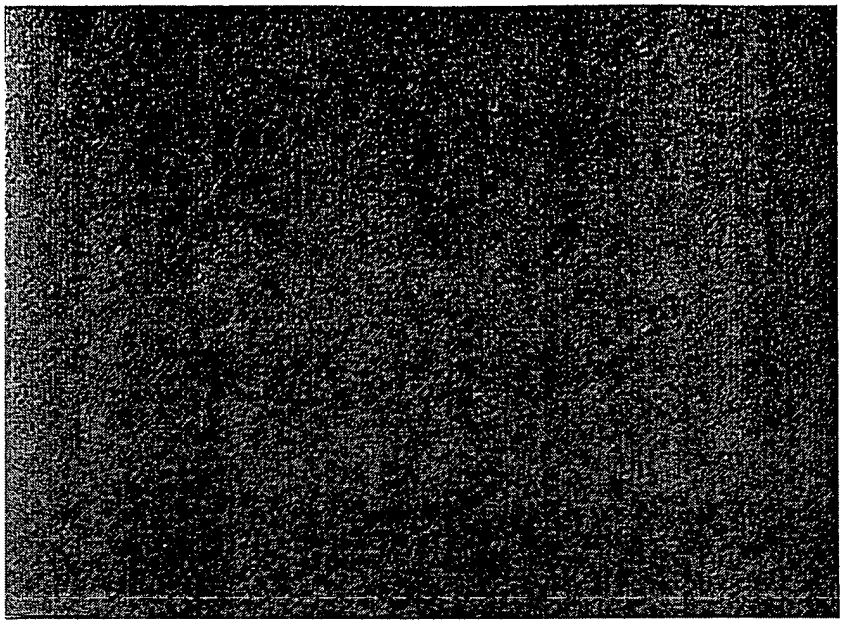


Fig. 5.1. Capacitance vs. Voltage results for the samples annealed at 1700°C for 40 min. with and without sacrificial oxidation.

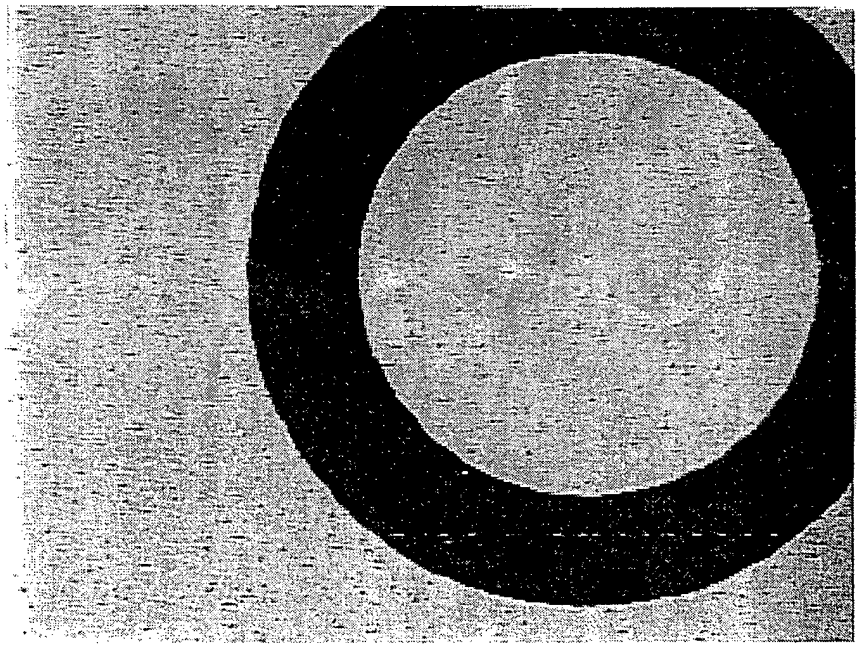
As seen in the figure, the C-V measurement taken right after the implant anneal without sacrificial oxidation results in a C-V curve that is noisy, with an undesired increase in capacitance at V >10V. The C-V measurement taken after sacrificial oxidation results in a curve that is smooth with more p-type characteristics. The first data was taken after the implant anneal. Following this a two step sacrificial oxidation was performed. After the implant anneal a dry oxidation was done at 1200°C for 30 min. in the Lindberg furnace to grow about 0.2μm. The oxide was etched off and another oxide was grown. A wet oxidation was done in the Blue-M oven at 1130°C for 2.5 hrs. in wet O_2 followed by an anneal in Ar for 0.5 hrs. This oxide of 0.35μm was also etched. A total oxide of about 0.45μm was grown and etched, which removed approximately 0.22μm of the semiconductor surface leaving a depth of 5.78μm of the implant region. By etching off the surface, the damage was minimized and any surface leakage current was reduced. The relatively smooth surface also improved the Schottky contacts, since the metal-semiconductor interface improved, and resulted in better C-V data.

The current-voltage (I-V) data displayed current in the 100μA range and 5μA range, at 20V, for the samples without and with sacrificial oxidation, respectively. Since the current decreased with the sacrificial oxidation, this indicates that the large current could be due to the surface damage that induced a surface leakage current. The increase in capacitance for V >10V may also be due to this leakage current.

The structure of the surface was also observed under high magnifications using the Nomarsky optical microscope, Olympus model BX60FM. From Fig. 5.2 the difference in the surface roughness is seen. The surface after the sacrificial oxidation, shown in Fig. 5.2 (c), is less rough than the surface after anneal with no sacrificial oxidation, shown in Fig. 5.2 (b). This suggests that the sacrificial oxidation reduces the surface damage. Initially this damage was assumed to be due to the ion implantation. However, when comparing the surface of the ion implanted sample prior to an anneal, in Fig. 5.2 (a), to that of the annealed sample, it is evident that the roughness is worse after the anneal. Therefore the roughness is not mainly due to ion implantation, which is known to damage the semiconductor surface and crystal structure, but the post-



(a)



(b)

implantation anneal.

The surface of the samples which were implanted at the same time but annealed at different temperatures was also investigated. Fig. 5.3 and 5.4 shows the surface of samples annealed at 1700°C, 1600°C, and 1500°C. The surface roughness increases with the anneal temperature. The trend of the damage is consistent with that observed due to step bunching [1]. Another factor could be that at high temperatures a dynamic step flow process during sublimation occurs which contributes to step bunching and results in the formation of macrosteps [14]. At higher temperatures this process would be more significant, therefore the damage seen in the figures could be due to these macrosteps.

5.2.2 Effect of Series Resistance

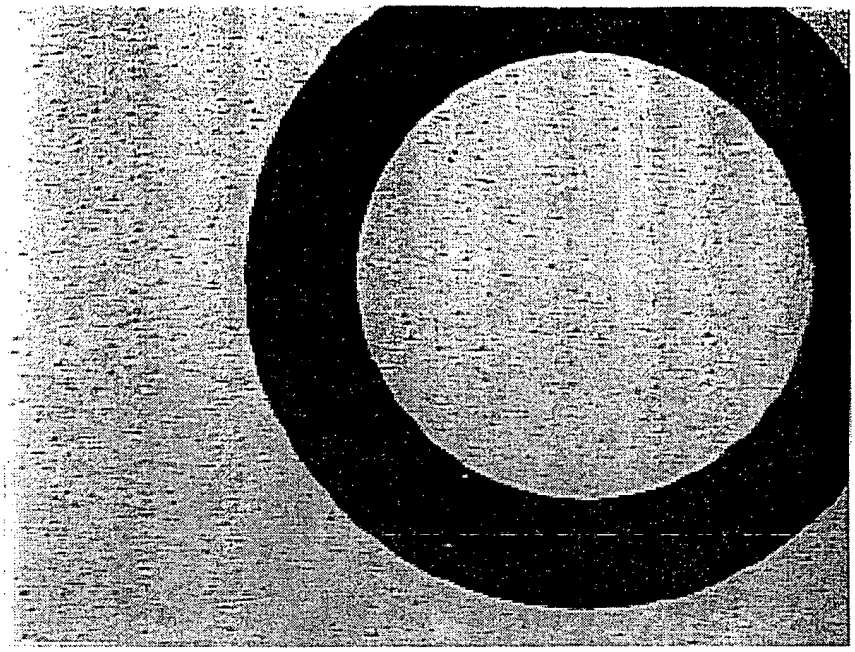
Ideally the capacitance should not change with frequency. However if there is a resistance in series with the depletion capacitance this would cause a significant shift in the capacitance characteristics measured at different frequencies. This capacitance frequency dependence is shown in Fig. 5.5. By modeling the device shown in Fig. 5.6, the impedance of the circuit model is derived as

$$Z = R_s + \frac{1}{G_p + j\omega C_p} \tag{5.1}$$

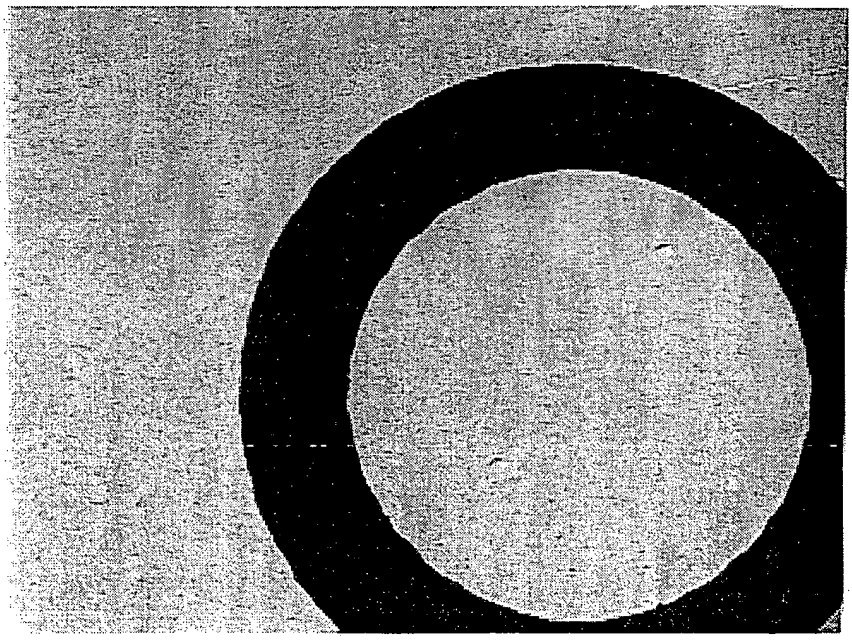
This model verifies that the frequency affects the value of the capacitance measured. It also indicates that at lower frequencies the capacitance impedance dominates and the series resistance can be assumed negligible. Therefore the C-V characteristics at lower frequencies represents the depletion capacitance more accurately.

5.2.3 Schottky C-V Characteristics

The increase in capacitance for V > 10V, seen in Fig. 5.1, may be due to surface leakage current. Similar increase in capacitance for V > 15V is also seen in the sample



(a)



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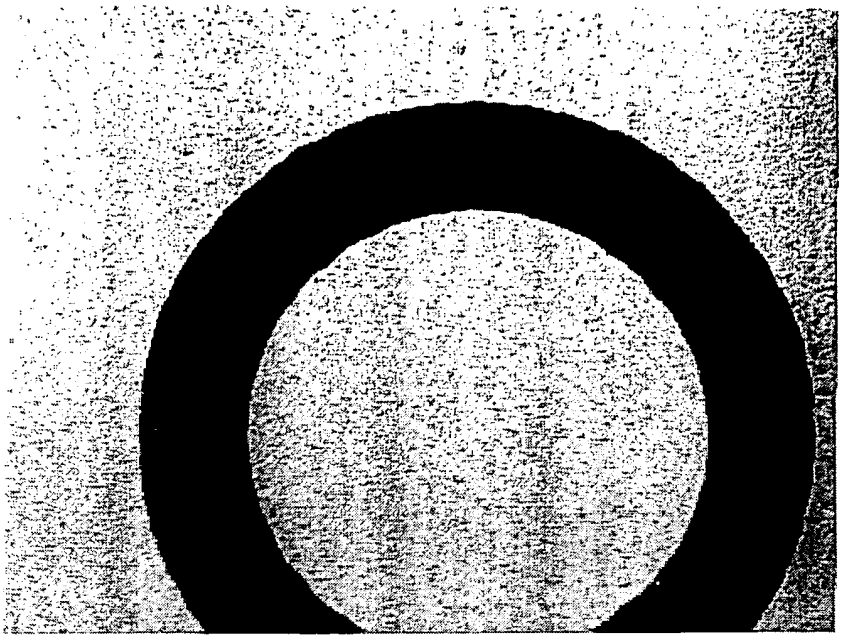
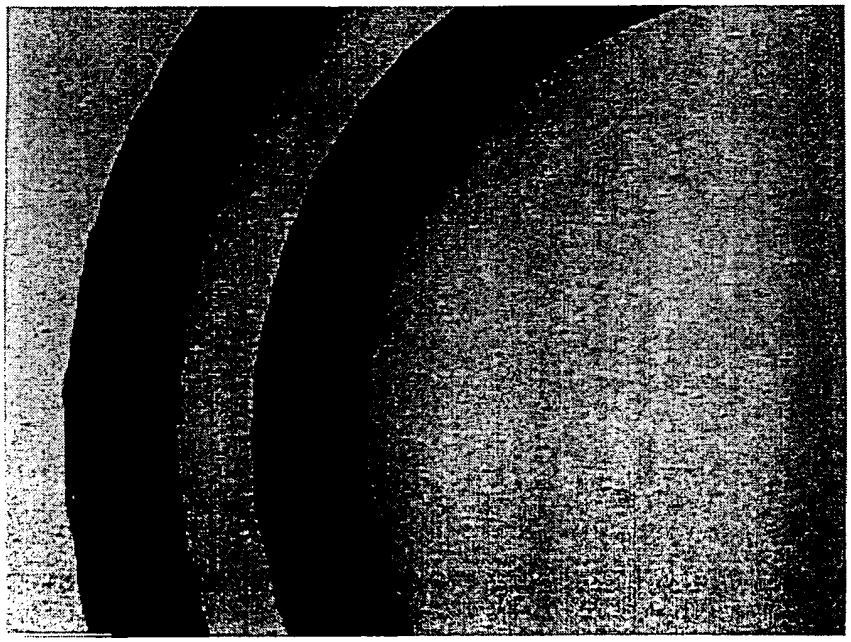
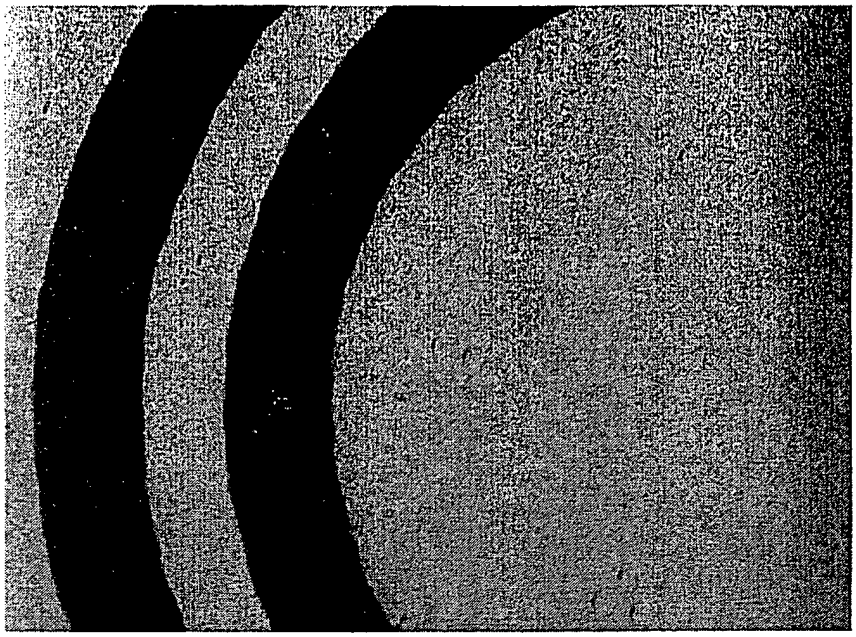


(c)

Fig. 5.3. Surface structure observed under a Nomarsky microscope, magnification 500x, without sacrificial oxidation annealed at (a) 1700°C, (b) 1600°C, and (c) 1500°C.



(a)



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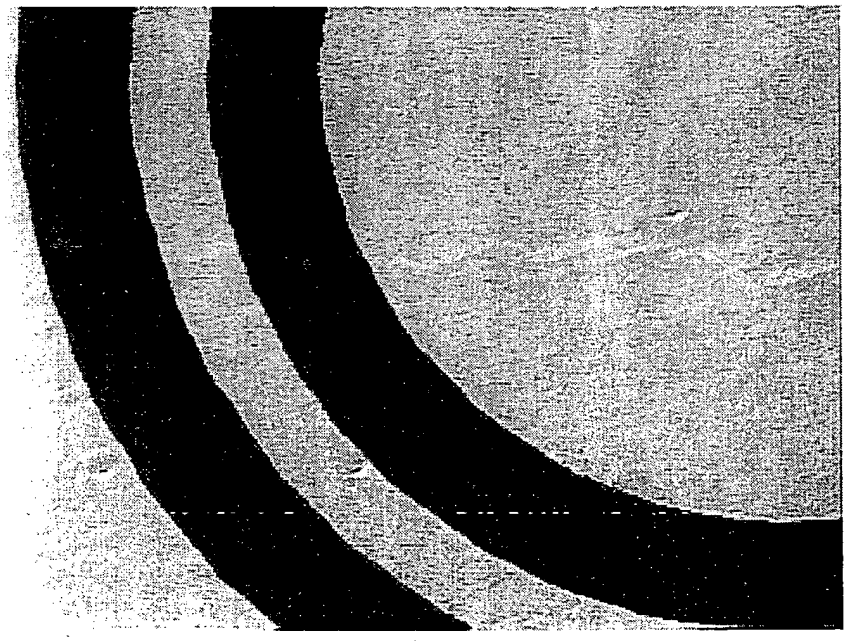


(c)

Fig. 5.4. Surface structure observed under a Nomarsky microscope, magnification 500x, with sacrificial oxidation at (a) 1700°C, (b) 1600°C, and (c) 1500°C.

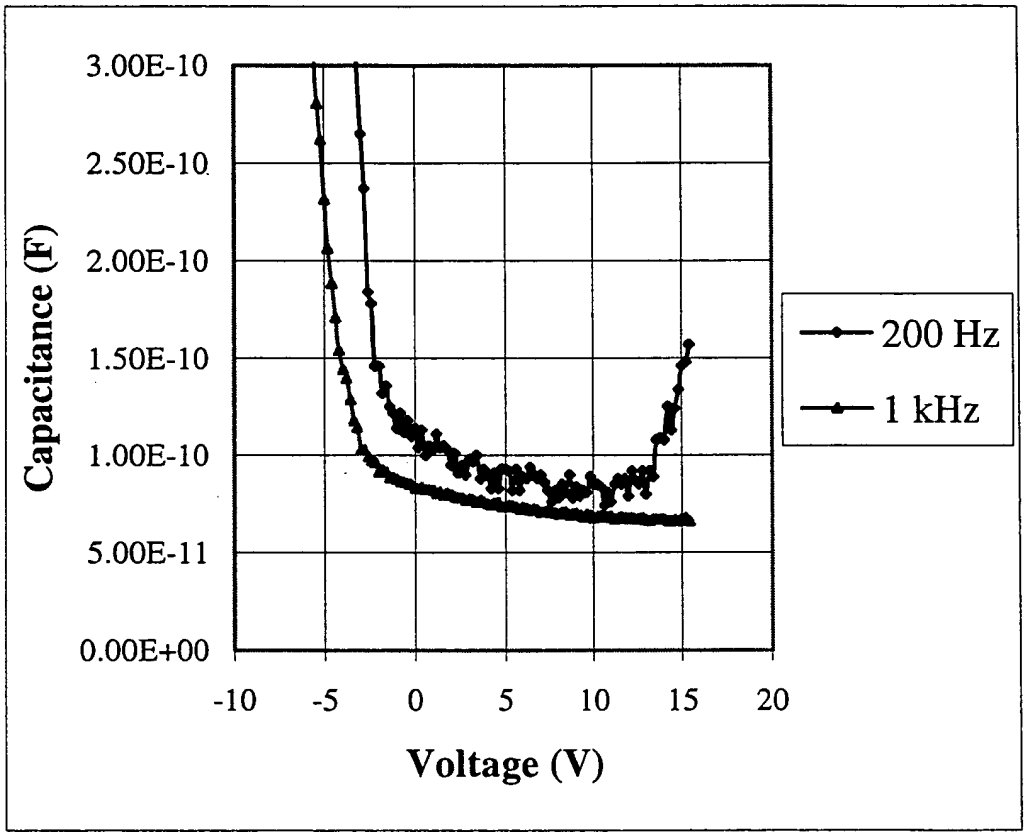


Fig. 5.5. Schottky C-V measurements, in the series mode, for different frequencies.

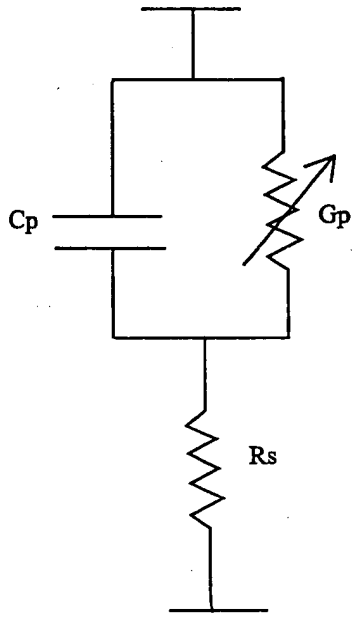


Fig. 5.6. Schottky device circuit model.

after sacrificial oxidation was performed leading to a reduction in the surface leakage current, Fig. 5.7, therefore the increase in capacitance is probably due to a strong image-force-induced lowering of the potential energy for charge carrier emission when an electric field is applied [39]. The minimum energy required for a hole to escape into the semiconductor is equivalent to the barrier height, Φ_{Bp}, of the metal, in this case for Ni. This value is very sensitive to surface contamination at the metal-semiconductor interface. When a hole is near the surface of the semiconductor it induces a negative charge on the metal contact. This negative charge or image charge causes an attractive force which is also called the image force. This force along with the electric field force causes a lowering of the Schottky barrier. At high fields the Schottky barrier is considerably lowered and the effective barrier for thermionic emission is reduced. This barrier lowering also has a profound effect on the current transport process where the current is mainly due to majority carriers. In forward bias conditions the current is controlled by the hole current flow from the semiconductor to the metal. In reverse bias conditions the current is controlled by the thermionic emission current flow from the metal to the semiconductor. Therefore the lowering of the barrier height due to field and image force results in an increase in the thermionic emission or reverse bias current. In addition, lowering of the barrier height due to contaminants, and the increase in the semiconductor doping could also increase the reverse bias current, resulting in a leaky contact. This increase in reverse bias current may have resulted in the increase in capacitance at high voltages where the electric field is stronger, shown in Fig. 5.7. To avoid this leakage current effect, the MOS capacitor technique is used to verify the activated doping of the implanted region.

5.3 MOS Capacitor Measurements

5.3.1 Effect of Series Resistance

Similar to the Schottky capacitor results, a frequency dependence of the

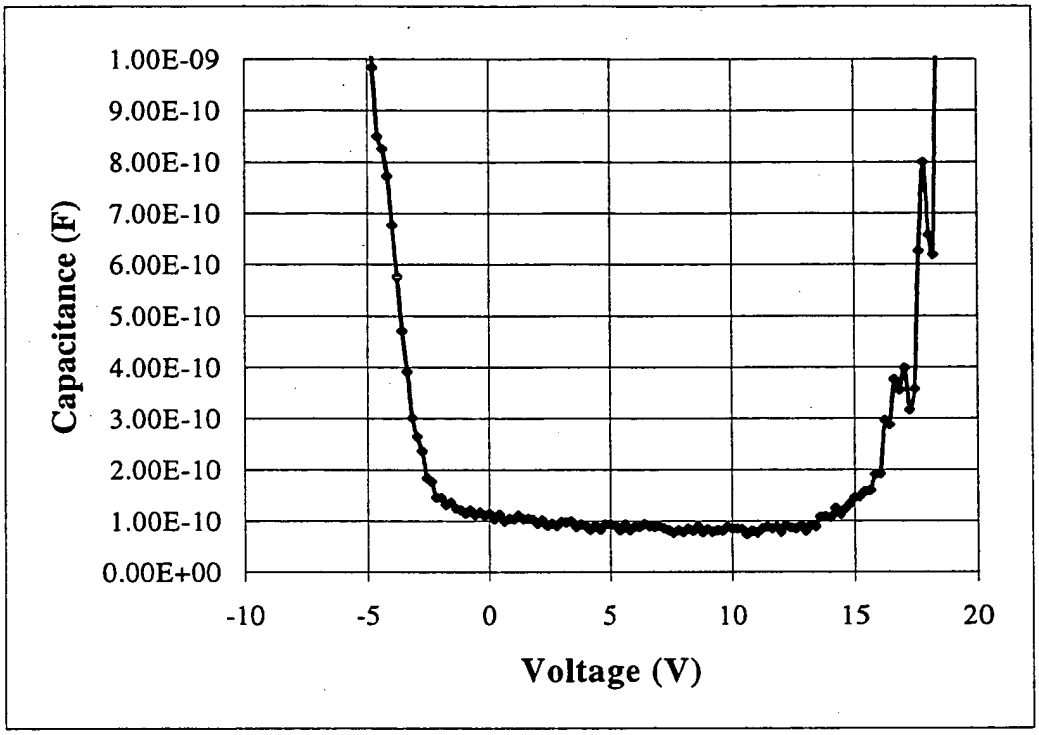


Fig. 5.7. Schottky C-V measurement, in the series mode, of an annealed sample with sacrificial oxidation.

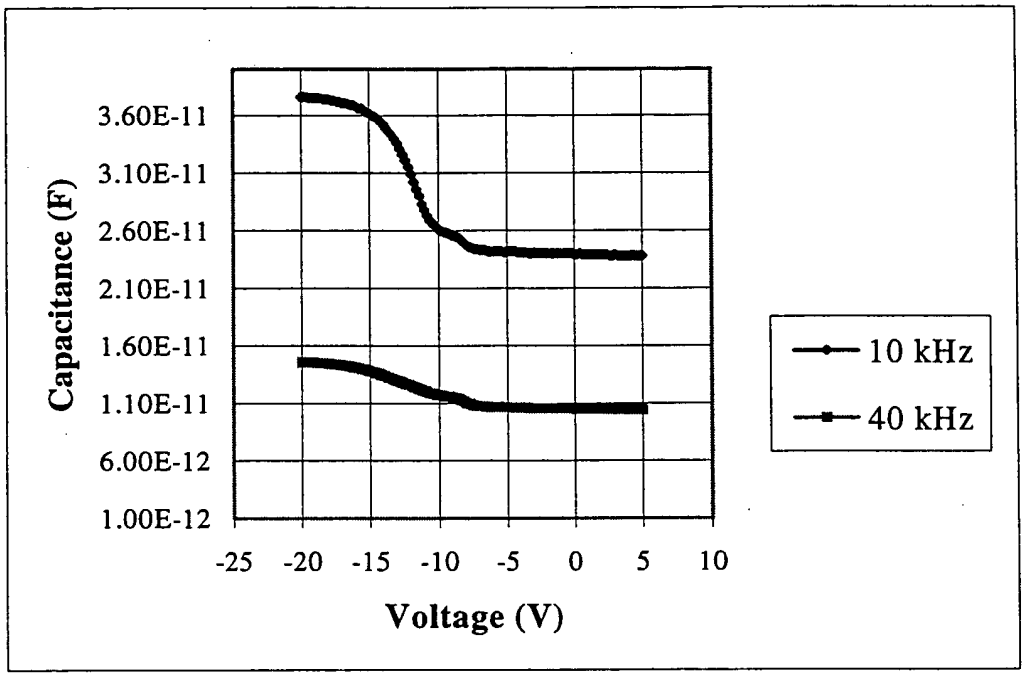


Fig. 5.8. MOS C-V measurements, in the parallel mode, for different frequencies.

capacitance measurements was observed as shown in Fig. 5.8. This again is attributed to the presence of series resistance. A similar circuit model as shown in Fig. 5.6 can be applied for the MOS device with the inclusion of the oxide capacitance in series. As noted before, this series resistance effect can be made negligible by going to lower frequencies. To eliminate the series resistance effect, the capacitance measurements were made quasi-statically at an effective frequency of 0.25 Hz.

5.3.2 Flatband Voltage Shift

A flatband voltage shift is usually attributed to oxide charge. An analysis of the C-V data measured indicated a significant shift of about -10V in the flatband voltage. This large negative flatband shift for SiC has been reported [40]. It has been attributed to fixed charge and holes trapped at deep states at the oxide-semiconductor interface. In Fig. 5.9 the lower curve shows the low-frequency C-V curve under dark conditions where a flatband shift of ~-10V was observed. Since the emission time of carriers from the deep states is extremely slow (over 1E10 years at RT) [41], holes trapped at the deep states behave like fixed charges, which result in the flatband shift being caused by both holes trapped at the deep states and fixed charges [40].

In Fig. 5.9 the upper curve shows the low-frequency C-V curve on which the illumination technique was used. This figure displays a voltage shift between the forward and reverse sweeps. This phenomenon has been previously reported and can be attributed to the density of charges at deep states [40]. After the bias is swept from accumulation to deep depletion in the dark, the device is illuminated. In this state the holes trapped at the deep states are emitted, resulting in the reduction of positive charges at the interface. Then as the bias is decreased the depletion layer narrows resulting in an increase in capacitance. Inversion is not observed since the power of the lamp did not provide a higher energy than the bandgap of SiC. If inversion occurred there would be an increase in capacitance after illumination, due to generation-recombination of minority carriers, remaining flat until the band bends toward accumulation causing the charge piled up at the oxide-semiconductor interface to move back into the semiconductor and result in a

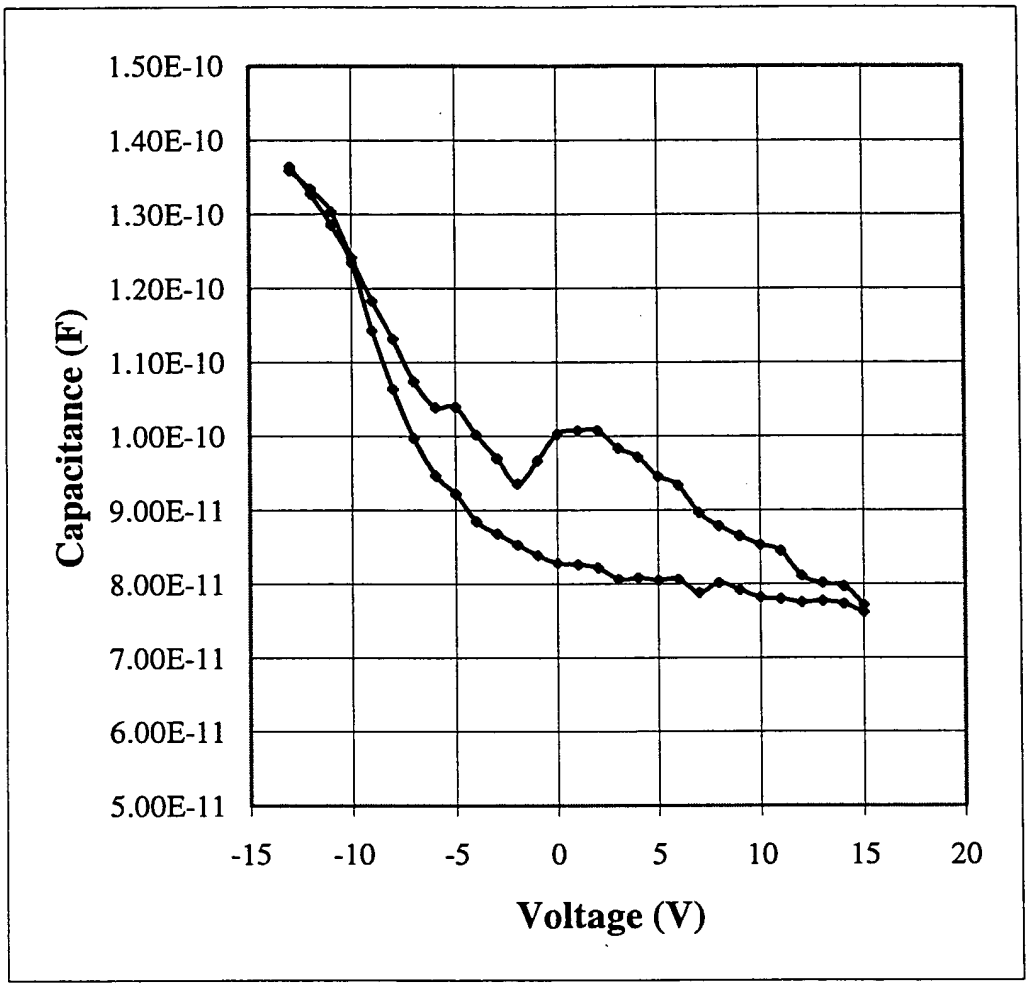


Fig. 5.9. Quasistatic MOS C-V measurements, in the parallel mode, swept from –13 to 15V, under dark, and then swept back after brief light illumination.

decrease in capacitance. This phenomenon was not observed in Fig. 5.9. In Fig. 5.9 as the bias is swept back, in the region between 15 and 2V the charge in the deep states remain neutral. This is because the charge in the state cannot change any more since the free carriers deplete from the interface in the valence band. In the region between 2 and – 13V the surface band bending flattens toward accumulation and holes appear near the interface in the valence band. This induces the deep states to capture these holes and change their charge state to positive. The captured holes are hindered from being thermally emmitted to the valence band due to the very slow emission rates. Since the charge state is neutral in the reverse sweep and positive in the forward sweep between 15 and 2V, this density of charges at deep states is reflected by the voltage shift at 2V.

5.3.3 Effect of Field Inversion

A field inversion layer can be formed in non-degenerately doped semiconductor regions which lie under areas covered by silicon dioxide over which no metal exists [42]. In the MOS capacitor this region would be the area between the gate and grid contact in Fig. 4.2. The lateral surface effects can influence the band-bending of the device at the surface, and nondegenerately doped semiconductors are easily influence by these effects. Field inversion can arise as a result of the potential on the surface of the oxide due to fringing field effects originating from the metal contact. The effects of this surface potential vary drastically depending on the humidity in the air, and they also vary as a function of time. This surface potential is usually caused by H+ and OH- ions which move around creating charge build-up at the surface of the oxide. This field inversion can supply carriers to form an inversion layer under the MOS capacitor, thereby affecting the capacitance characteristics. Since the potential is affected by humidity, the act of blowing dry N_2 over the oxide increases the sheet resistance and reduces the relative humidity. Therefore the effect of the field inversion layer on the capacitance characteristics can be observed by taking C-V measurements with and without blowing dry N_2 over the sample.

To verify if field inversion did occur, the data was taken after initially biasing the capacitor to accumulation, so positive ions would accumulate at the oxide surface, and blowing nitrogen over the device for a short while. This process freezes the ions accumulated at the oxide surface adjacent to the metal, preventing the field inversion effect. The capacitance measurement shown in Fig. 5.10 shows no inversion characteristics in the measurement taken without dry N_2 blown as compared to with dry N_2 blown over the oxide surface. Therefore this suggests that field inversion did not occur. The shift in the oxide capacitance is probably due to oxide charge.

5.4 Interpretation and Comparison of Activation Results to Current Findings

5.4.1 Effect of Anneal Temperature

The effect of anneal temperature of 1500°C, 1600°C, and 1700°C on boron implantations into n-type 6H, with dose concentration of 2.65E14 cm^{-2}, and into n-type 6H and 4H, with dose concentration of 1.3E15 cm^{-2}, is shown in Fig. 5.11 (a), (b) and (c), respectively. The MOS C-V measurements, shown in these figures, show an increase in the depletion capacitance as the anneal temperature increases. This increase in the depletion capacitance with temperature indicates an increase in the doping concentration. By using a second order polynomial fit to calculate the $1/Cdep^2$ slope, the doping concentration was extracted. The doping for each of the implantations, shown in Fig. 5.12, 5.13, and 5.14, verified the increase in the doping concentration with anneal temperature. The difference in the doping concentration with depth could be due to the variations in the implantation profile, which was not completely flat at all depths. The activation percentage extracted for the 6H-SiC with total dose of 2.65E14 cm^{-2} at depletion depths of 1E-6 to 1.2E-5 cm is 15-19.3%, 21.3-28.3% and 30-36% for the anneal temperatures of 1500°C, 1600°C, and 1700°C, respectively, as shown in Fig. 5.15 (a). Using similar extraction methods the activation percentage for the 6H-SiC with total dose of 1.3E15 cm^{-2} at depth of 2E-6 to 7E-6 cm is 9.3-14.7%, 11.3-16% and 15.3-36.7% for the anneal temperatures of 1500°C, 1600°C, and 1700°C, respectively, as shown in

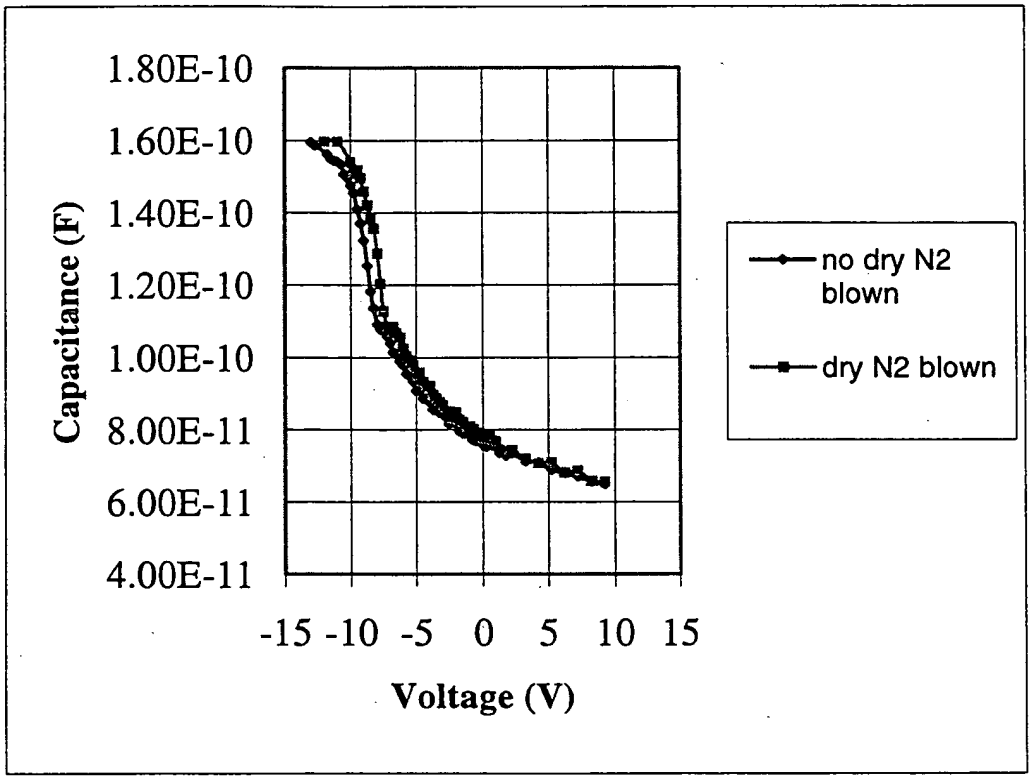
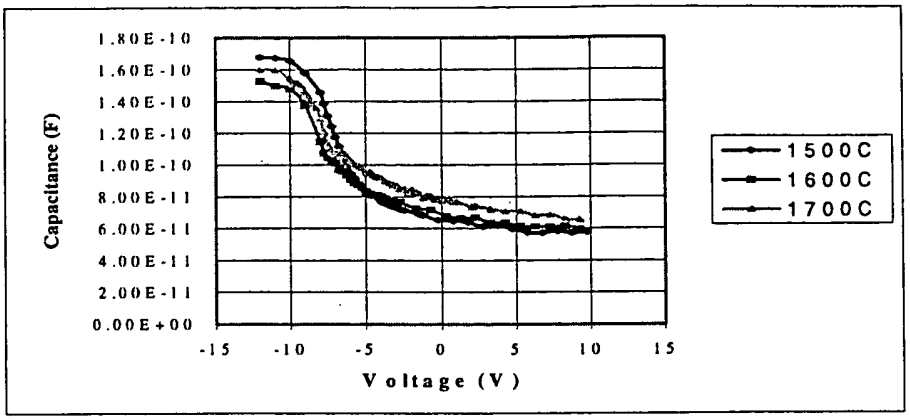
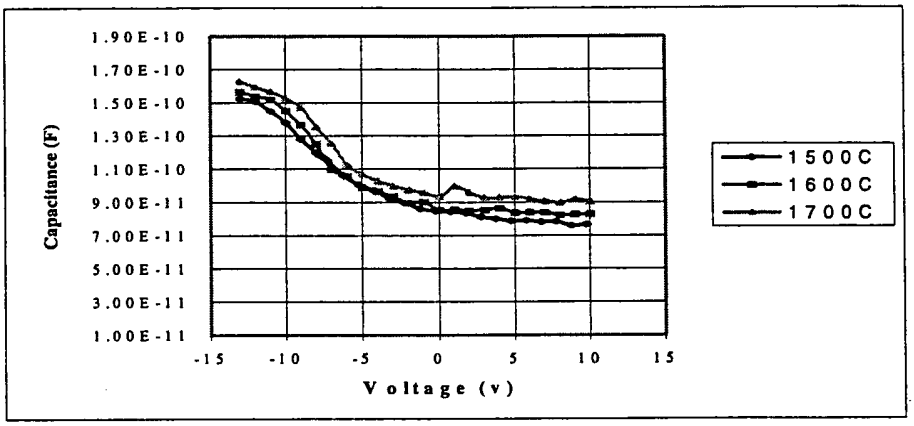


Fig. 5.10. MOS C-V measurements before and after blowing nitrogen over the device while it was biased at accumulation.



(a)



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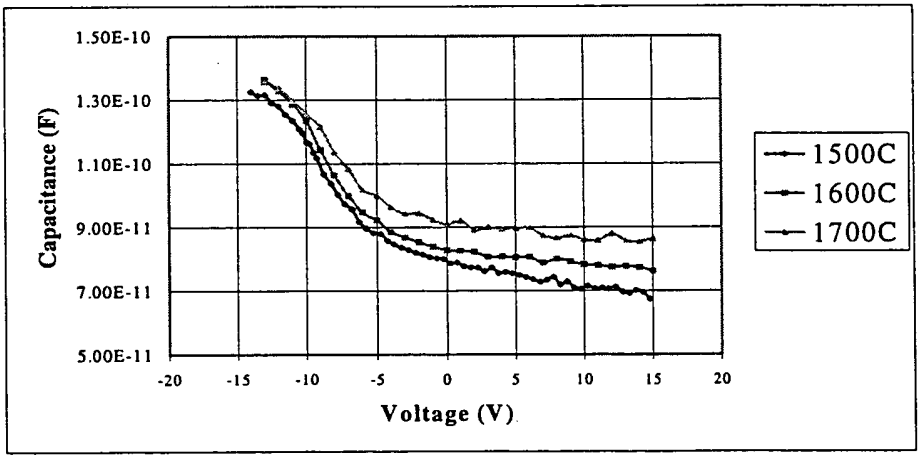


(c)

Fig. 5.11. Quasistatic MOS C-V measurements for B implantations into n-type (a) 6H-SiC with a total dose of 2.65E14 cm^{-2}, (b) 6H-SiC with a total dose of 1.3E15 cm^{-2}, and (c) 4H-SiC with a total dose of 1.3E15 cm^{-2}.

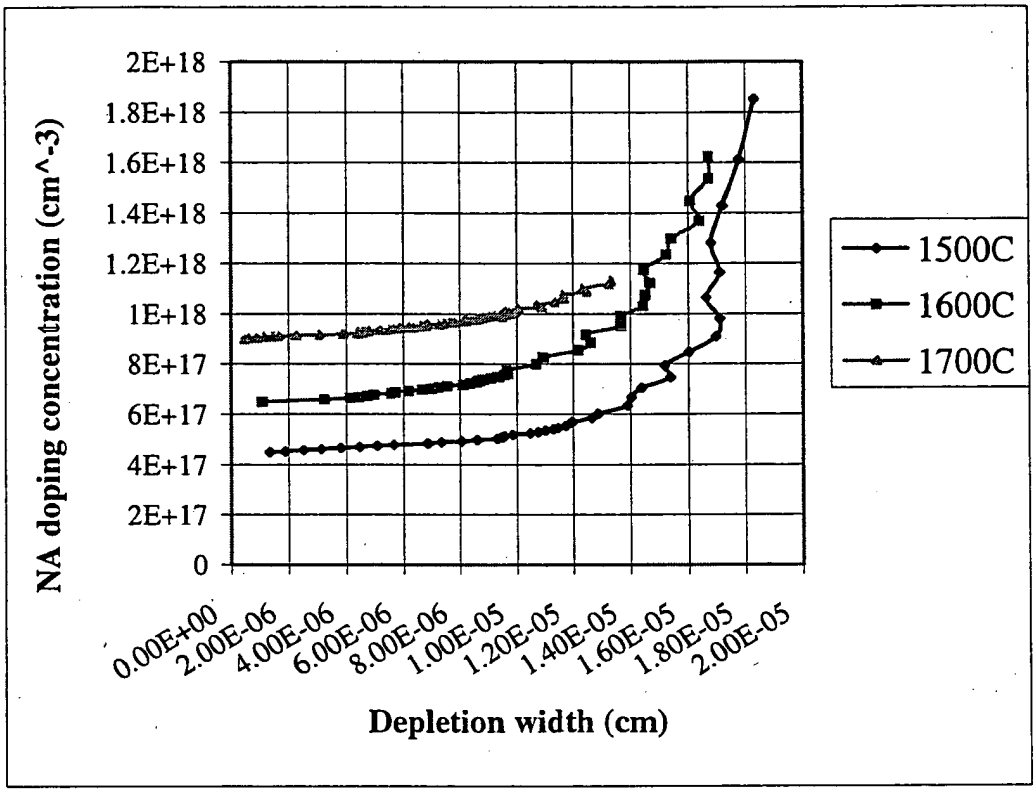


Fig. 5.12. Doping concentrations vs. depletion depth for B implantations into n-type 6H-SiC with a total dose of 2.65E14 cm^{-2} annealed for 40 min. at anneal temperatures of 1500°C, 1600°C, and 1700°C.

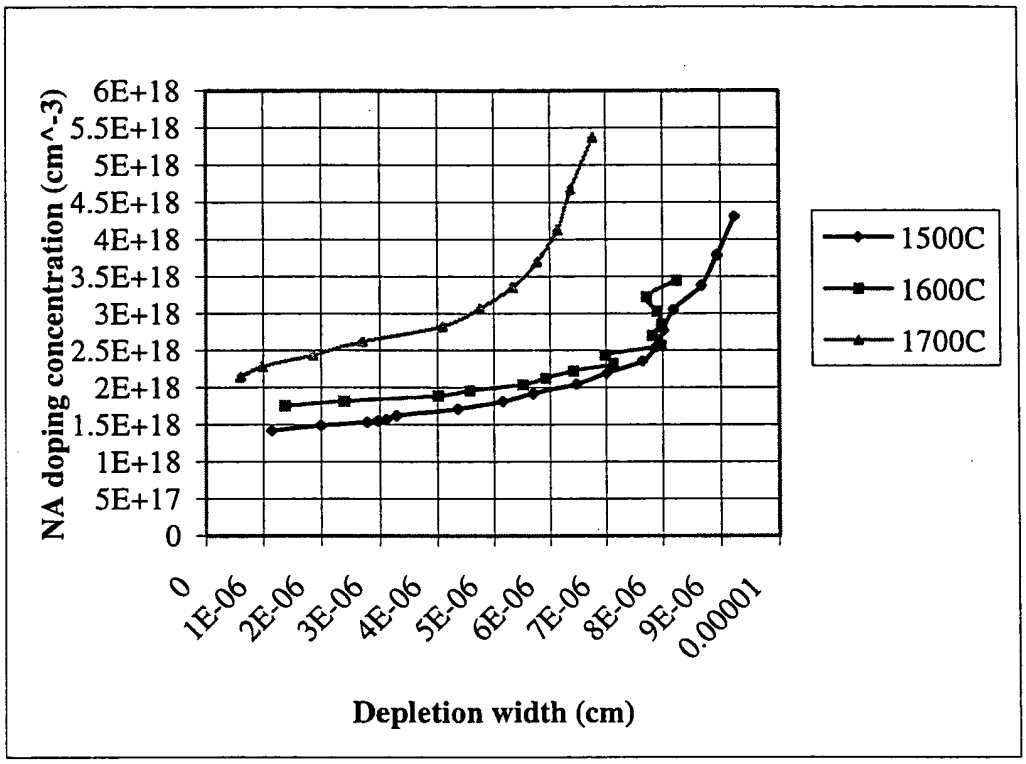


Fig. 5.13. Doping concentrations vs. depletion depth for B implantations into n-type 6H-SiC with a total dose of 1.3E15 cm^{-2} annealed for 40 min. at anneal temperatures of 1500°C, 1600°C, and 1700°C.

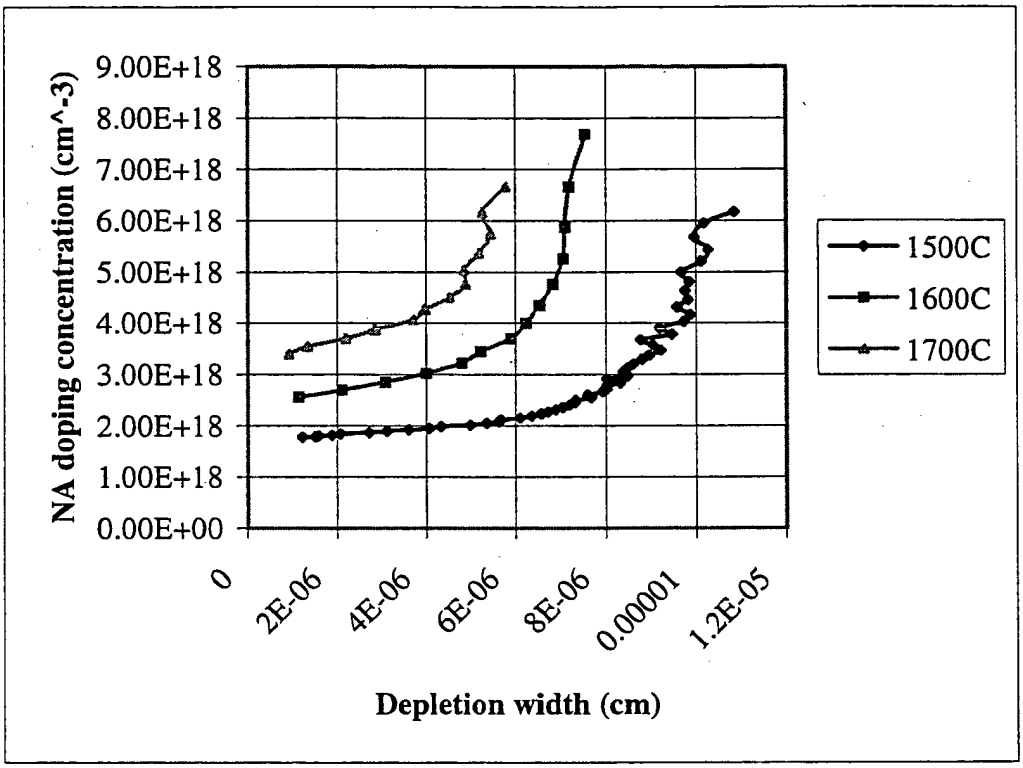
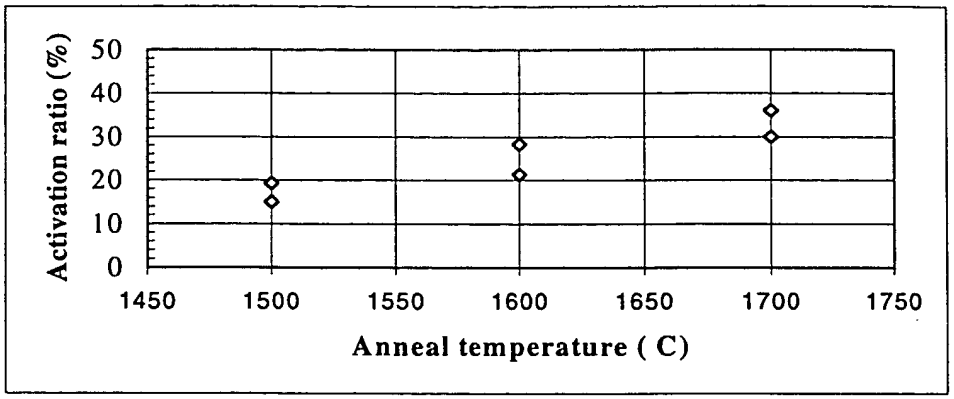
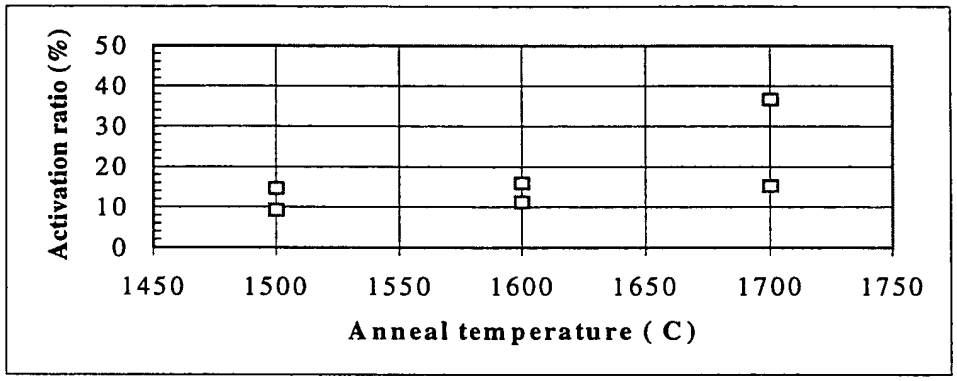


Fig. 5.14. Doping concentrations vs. depletion depth for B implantations into n-type 4H-SiC with a total dose of 1.3E15 cm^{-2} annealed for 40 min. at anneal temperatures of 1500°C, 1600°C, and 1700°C.



(a)



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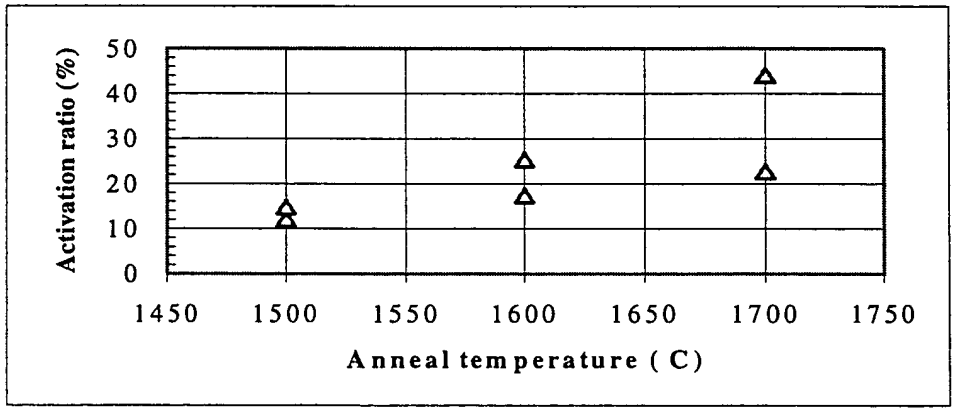

(c)

Fig. 5.15. Activation ratios vs. anneal temperatures for B implantations into n-type (a) 6H-SiC with a total dose of 2.65E14 cm^{-2}, (b) 6H-SiC with a total dose of 1.3E15 cm^{-2}, and (c) 4H-SiC with a total dose of 1.3E15 cm^{-2}.

Fig. 5.15 (b). Finally the activation percentage obtained for the 4H-SiC with total dose of 1.3E15 cm^{-2} at depths of 1E-6 to 6E-6 cm is 12-14.7%, 17.3-25.3% and 22.7-44% for the anneal temperatures of 1500°C, 1600°C, and 1700°C, respectively, as shown in Fig. 5.15 (c). The increase in activation with temperature may be attributed to the fact that higher temperatures impart more energy for SiC atoms to move back to the lattice sites, ameliorating the damage to the crystal structure. The higher energy could also facilitate B atoms to occupy Si sites, which would result in an augmented acceptor concentration and coincide with the higher activation ratio. It is desirable to get B on the Si lattice sites, as opposed to the C site, beacause it is the shallower of the acceptor level. The activation also increased with depth, for which a possible explanation could be that at shallower depths more damage exists, because of the implantation process, resulting in the shallower damaged region being more difficult to activate than the deeper less damaged region.

5.4.2 Effect of Implant Dose

Results of B implantations into the same polytype 6H-SiC and anneal conditions, but different implant dose concentrations are shown in Fig. 5.16. A slight drop in the activation ratio is noticed at the higher concentration. This could be because high implant doses cause more ions to be bombarded into the material, resulting in a higher probability of defect formation. The B-related defect centers called "D-center", which are presumed due to B atoms residing in C lattice sites and neighbouring intrinsic defect such as a Si vacancy [17], could be formed. It is known that these defect centers are donor-like, therefore they would compensate the activated acceptor concentration resulting in a reduction of acceptor activation ratio

It is also observed that at lower doses the activation doesn't vary too much with depth as compared to the heavier dose implant. This could be that the damage at shallower depths for higher doses is worse as more ions are bombarded into the sample. The shallower depth regions would therefore be more difficult to activate than the deeper depths, resulting in the notable variation in activation ratio with depth.

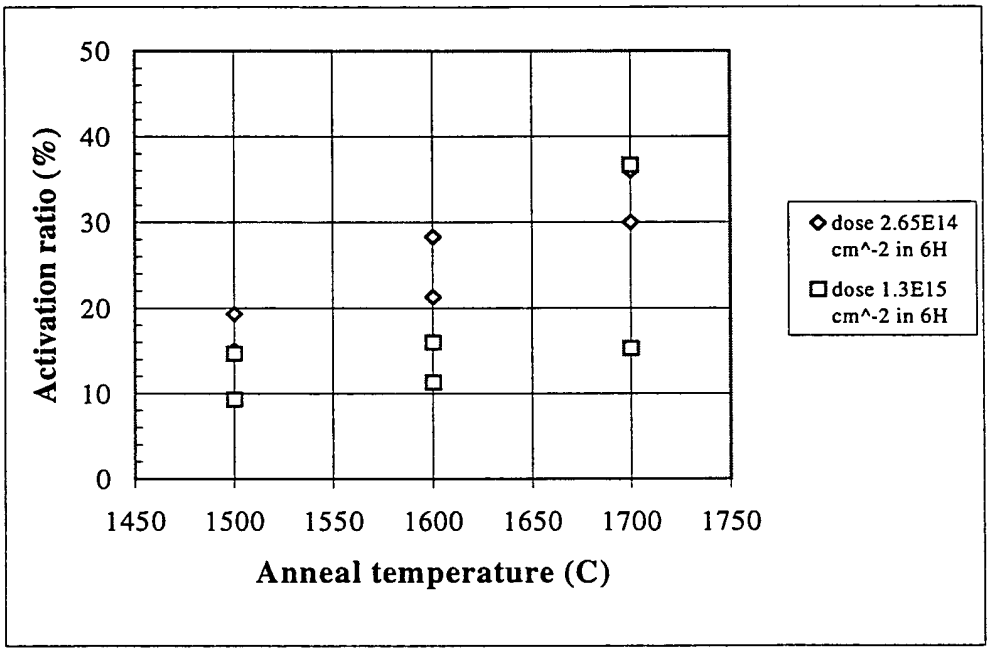

Fig. 5.16. Activation ratios vs. anneal temperatures for B implantations into n-type 6H-SiC but different implant dose concentrations of 2.65E14 cm^{-2}, and 1.3E15 cm^{-2}.

5.4.3 Effect of Polytype

Implants with the same dose concentration into two polytypes, 6H and 4H, were investigated. Fig. 5.17 shows the activation ratio vs. anneal temperature for 6H and 4H polytype, both implanted with a dose of 1.3E15 cm^{-2}. It is seen that 4H is slightly better activated than 6H. This could imply that the implantation-induced damage is worse in 6H than 4H.

5.4.4 Comparison of Activation Results to Current Publishings

The activation results obtained are compared to previous activation results obtained by M. A. Capano et al. [14] and T. Kimoto et al. [8] in Fig. 5.18. It is seen that at the temperature of 1500°C and 1600°C approximately the same activation was obtained in all three studies cases. However at 1700°C a factor of ~3 improvement was observed by M A. Cpano et al., and a factor of 5 improvement was observed by T. Kimoto when compared to the activation results found in this study. To account for this discrepency the experiment techniques were compared.

In the experiments done by M. A. Capano the anneal conditions used were the same as in this study. In both cases the anneals were done in an Ar ambient for 40 min. using the same resistively-heated furnace at the Air Force Research lab. The difference was in the implant profiles used. The previous results were obtained for a retrograde implant profile, shown in Fig. 5.19, while in this study a box profile was used. A possible explanation could be that diffusion occurred at higher temperatures. Since a retrograde implant was used, the large peak at the depth of 600 nm could have diffused into the shallower regions due to the concentration gradient. Also if more damge existed near the surface, because of the implantation process, this might also enhance the diffusion towards the surface. If diffusion did occur, then the activation ratio in the Capano study would be lower than calculated by those authors. To obtain the same activation ratio of ~22% in both cases, the doping concentration of the retrograde implant at 100 nm would be greater than the implanted 1E18 cm^{-3}. Therefore the 66% of 1E18

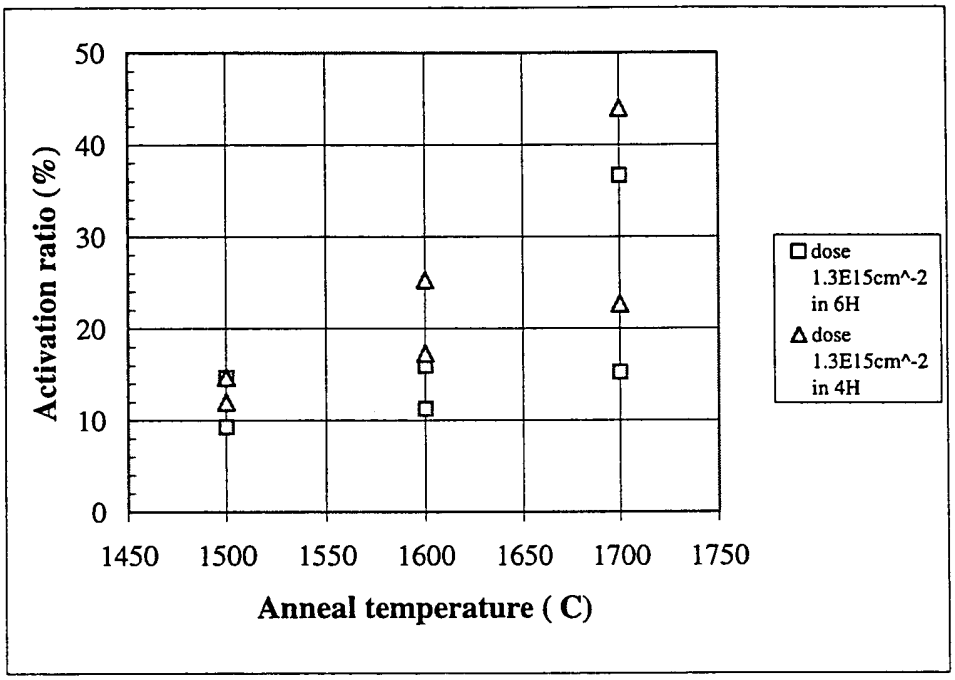

Fig. 5.17. Activation ratios vs. anneal temperatures for B implantations with dose 1.3E15 cm^{-2} for polytypes 6H and 4H-SiC.

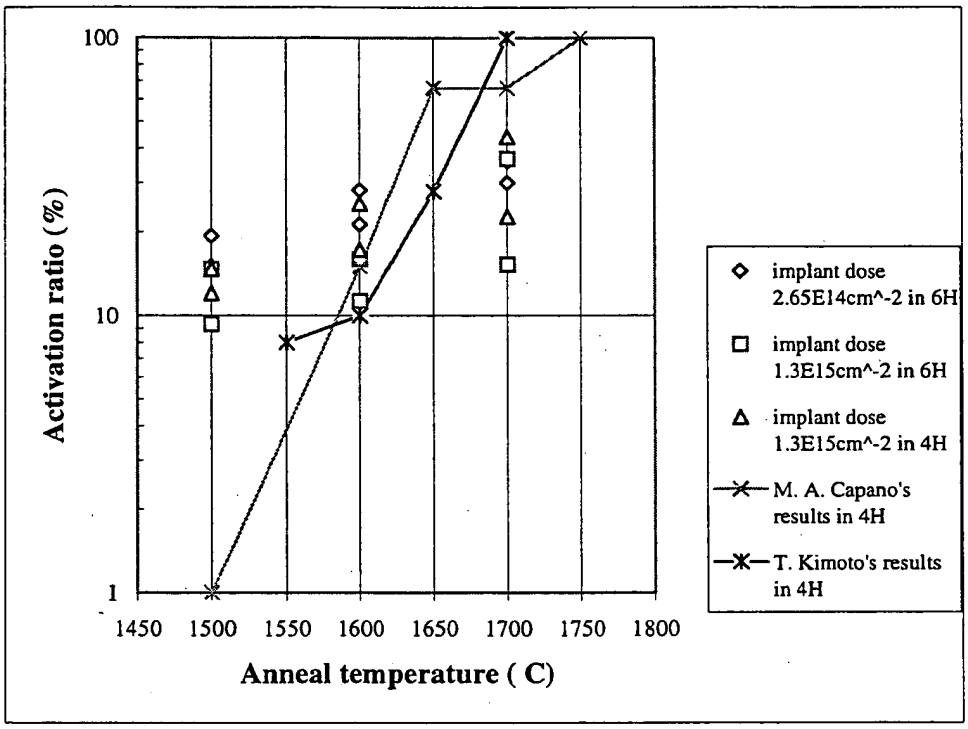

Fig. 5.18. B implantation activation ratios vs. anneal temperatures of results in this study and previously recorded results on n-type 4H-SiC and 6H-SiC [14,8].

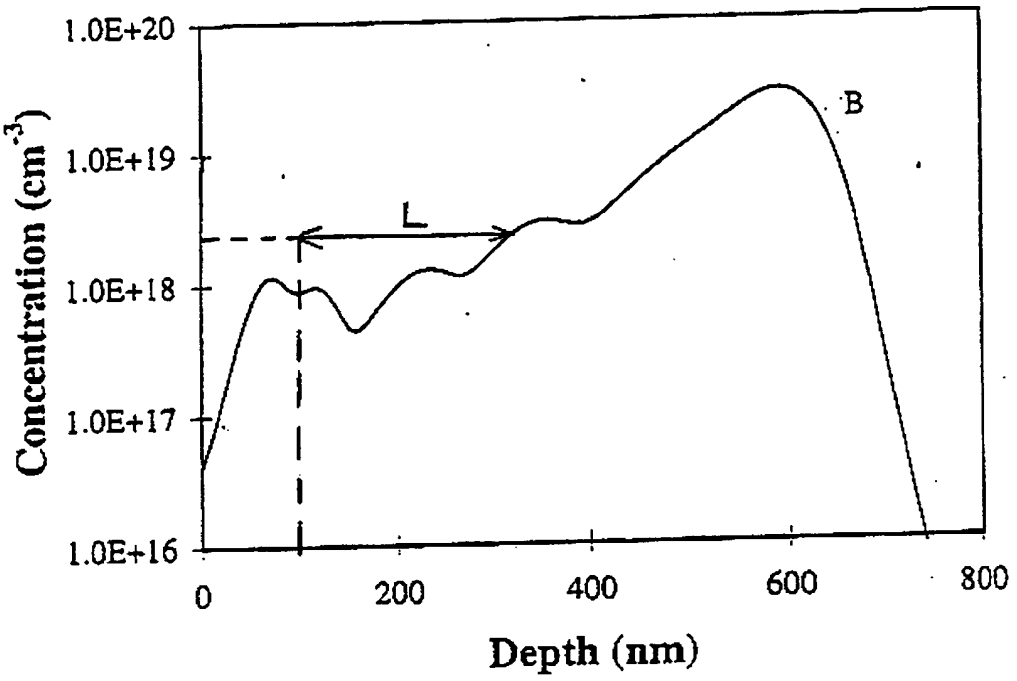

Fig. 5.19. B implant profile of the retrograde implant on n-type 4H-SiC done by M.A. Capano [14].

cm^{-3} doping concentration would correspond to a 22% activation of 3E18 cm^{-3} concentration. By looking at the plot in Fig. 5.19, this would correspond to a diffusion of 300 nm. Assuming this as the diffusion length, the diffusion coefficient is calculated. The calculation is shown below

$$D = \frac{L^2}{t} = \frac{\left(3 \bullet 10^{-5} cm\right)^2}{2400 \sec} = 3.7 \bullet 10^{-13} \frac{cm^2}{\sec} \tag{5.1}$$

where L is the diffusion length, and t is the anneal time of 40 min. This is a large diffusion coefficient for SiC. Similar diffusion has been observed with SIMS, leading to a broadening of the implanted profile and an outdiffusion of B acceptors, at an anneal temperature of 1700°C for 30 min [16]. The diffusion coefficient has been estimated to be 8.3E-13 cm^2/s [16] which correspond to the large value obtained in (5.1). This diffusion coefficient was estimated from the out diffusion. Similar large diffusion coefficient values have been observed at Cree Research. Therefore diffusion of impurites may account for the discrepency in the results.

In the experiments done by T. Kimoto et al., a box implant profile was used with a total dose concentration of 1E14 cm^{-2}. SIMS was done on the annealed samples and no significant diffusion was observed, therefore the diffusion theory would not explain the discrepency. The anneals were also done in an Ar ambient, but for a slightly shorter time of 30 min. as compared to 40 min. A different furnace was used, which might have caused the discrepency between the results. If the furnace was not calibrated accurately, then the temperature measured to the actual temperature of the sample during anneal may have been different. If the anneal temperature was actually at 1750°C or 1800°C, this would cause notable difference in the activation. An increase in the activation of temperatures from 1700°C to 1750°C was also seen in the previous compared literature. It was reported that batch-to-batch reproducibility was relatively poor [43]. This could be attributed to the fluctuation of annealing temperature. It is also noted that the implant dose was a factor of nearly 3 or more less than that used in this study. This may have

also been an element which leads to the higher activation ratio. The lower dose may cause less implant damage and consequently increase the percentage activated. Another possibility may be that the effect of series resistance may not have been minimized, since the data was measured at a frequency of 100 kHz [43], which gave rise to higher capacitance measurements and therefore higher activation ratios.

CHAPTER 6

CONCLUSIONS & RECCOMENDATIONS

6.1 Conclusion

The purpose of this research is to study the activation of boron ion implantations in both 6H and 4H-SiC. The effect on the activation for different parameters was analyzed and compared. One parameter changed was the implant anneal temperature. Three different temperatures of 1500°C, 1600°C, and 1700°C were used. The CV curves were measured on Schottky capacitors and MOS capacitors. The activation ratios were then extracted from the MOS CV measurements. The surface structures using an optical microscope for the different anneal temperatures were also observed. Another parameter varied was the implant dose. Two different total doses of 2.65E14 cm^{-2} and 1.3E15 cm^{-2} were implanted into 6H-SiC. The activation ratios were then extracted from MOS CV measurements. A third parameter changed was the polytype. A total dose of 1.3E15 cm^{-2} was implanted into both 4H and 6H-SiC. The activation ratios were again calculated from MOS CV measurements.

Several conclusions were drawn from the CV measurements. It was exhibited that both MOS and Schottky CV measurements varied significantly with frequency, indicating series resistance. It was shown that low frequency measurements minimized this series resistance. In the Schottky C-V curves it was noted that surface damage played an important role in the quality of the contact. It was recognized that sacrificial oxidation considerably improves the Schottky contact and surface structure. From the

surface structures inspected it was revealed that the anneal temperature also affected the surface roughness. It was noted that higher temperature anneals resulted in a more nonplanar surface. The nonplanarity also resulted in leaky Schottky contacts, therefore MOS C-V curves were considered more accurate in extracting the activation ratio. In the MOS C-V curves a significant flatband voltage shift was observed, which is attributed to fixed charges at the oxide-semiconductor interface and holes trapped at deep states at the interface. The characteristics pertaining to field inversion was not observed when dry N_2 was blown over the sample, therefore it is concluded that field inversion did not occur.

Several conclusions were also drawn from the activation ratios obtained. The activations obtained for implant dose of 2.65E14 cm^{-2} in 6H-SiC at anneal temperatures of 1500°C, 1600°C, and 1700°C were 15-19.3% , 21.3-28.3%, and 30-36%, respectively. For implant dose of 1.3E15 cm^{-2} in 6H-SiC the activations at anneal temperatures of 1500°C, 1600°C, and 1700°C were 9.3-14.7%, 11.3-16%, and 15.3-36%, respectively. Lastly for implant dose of 1.3E15 cm^{-2} in 6H-SiC the activations at anneal temperatures of 1500°C, 1600°C, and 1700°C were 12-14.7%, 17.3-25.3%, and 22.7-44%, respectively. Higher implant anneal temperatures improve the activation rate. This is attributed to the increase in thermal energy for the amendment of the crystal structure and the facilitation of the occupation of B atoms at the Si lattice sites. It is also seen that higher implant doses reduce the activation percentage. The reason for this is suspected to be due to the increase in implant damage at higher doses, which ensues in a harder activation of the implanted regions. Implant damage is also believed to be the cause of the increase in the activation ratio with depletion depth. At shallower depths more damage exists, reducing the ability for activation. At deeper depth less damage exists, leading to the easier activation of B. Another observation is the improvement in the activation between 6H and 4H polytypes of SiC.

The activation results were also compared to current results and the discrepancies were attributed to several factors. The difference in implant dose concentrations may have been the grounds for the disagreement in the activations obtained. Another factor could be the difference in the implant profiles, which may have resulted in occurrence of

diffusion at higher anneal temperatures. The accuracy of the anneal temperatures could also be the cause. Another reason may be the difference in the measurements techniques.

6.2 Recommendations

Further research on the activation of boron ion implants into SiC could provide a much clearer picture on the properties studied here. To verify if activation further improves with implant anneal temperatures, the measurements can be done on samples annealed at 1750°C and 1800°C. The effect of implant dose can also be investigated further by performing similar experiments as in this study on samples of the same polytype implanted with several different doses. The activation rate variation with polytype can be investigated by implanting samples of different polytypes with the same implant dose. To verify the cause of activation improvement with depletion depth, Rutherford backscattering methods can be used to analyze the surface damage at different depths. The effect of diffusion at higher anneal temperatures can also be explored more by performing SIMS on samples before and after implant anneals. In addition, anneal time dependent studies could also be conducted at each temperature.

Subsequent techniques in the improvement of the activation of boron can be considered. Coimplantation with C has been perceived to enhance the activation ratio of boron. Studies using C-coimplantation of various C to B implant ratios could be executed on both 4H an 6H SiC. Investigation into the best anneal ambient could be pursued. It has been reported that a silane anneal ambient produces better activations, therefore experiments using this ambient could be performed. The effect of implant temperature could also be analyzed.

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APPENDIX

SCHOTTKY & MOS DEVICE FABRICATION RUN SHEET

1. New sample clean _____

Soak in Acetone (ACE)	3 min.
Soak in Methanol (METH)	3 min.
Blow dry with N2	
Soak in aqua regia (1 HCL:1 HNO_3)	15 min.
Pour out aqua regia	
Rinse in De-ionized (DI) water	30 min.

2. General purpose oxidation clean _____

Soak in buffered oxide etch (BHF)	5 min.
Rinse in DI	1 min.
Soak in piranha (1 H_2O_2:1 H_2SO_4)	15 min.
Rinse in DI	6 times
Blow dry in N_2	

3. Oxidation _____

Dry oxidation in Lindeberg
1200°C 30 min.

4. Send for ion implantation _____

Species: Boron
Temperature: 650°C
Implant angle: 0°C
Beam current: 50 mA
Energies and doses for
batch 1 implant 1:
5.5E12 cm^{-2} at 20 keV
1E13 cm^{-2} at 52 keV
1.6E13 cm^{-2} at 110 keV
2.7E13 cm^{-2} at 200 keV
batch 1 implant 2:
9E12 cm^{-2} at 15 keV
1.7E13 cm^{-2} at 40 keV
3E13 cm^{-2} at 90 keV
4E13 cm^{-2} at 170 keV

1.1E14 cm^{-2} at 300 keV

batch 2 implant 1:

7E13 cm^{-2} at 15 keV

1.4E14 cm^{-2} at 45 keV

2.2E14 cm^{-2} at 100 keV

3.2E14 cm^{-2} at 180 keV

5.6E14 cm^{-2} at 300 keV

5. Sawing SiC wafer _____

Mount sample on carrier (glass plate) using photoresist	
Spin resist (AZ 1518) on carrier	1000 RPM 10 sec.
Spin resist on sample for protection	1000 RPM 10 sec.
Place sample on carrier	
Hardbake photoresist	120°C 15 min.
Score sample using diamond saw	

6. Strip Photoresist _____

Soak in ACE to remove resist	5 min.

7. Solvent Clean _____

Soak in ACE	3 min.
Soak in METH	3 min.
Blow dry with N2	

8. Post-Implantation clean _____

Soak in aqua regia	15 min.
Pour out aqua regia	
Rinse in DI	30 min.
Soak in $HF:HNO_3$ (1:1)	15 min.
Rinse in DI	6 times
Soak in piranha	15 min.
Rinse in DI	6 times
Blow dry in N_2	

9. Send for implant activation _____

Anneal samples in a resistively-heated furnace

In an Argon ambient at Airforce Research labs

Sample 1: 1500°C 40 min.

Sample 2: 1600°C 40 min.

Sample 3: 1700°C 40 min.

10. Oxide etch and clean sample _____

Soak in BHF	5 min.
Rinse in DI	1 min.
Soak in piranha	15 min.
Rinse in DI	6 times

For Schottky devices go to step 14

For MOS devices follow steps 11-13 and then continue from step 15

11. RCA clean _____

Soak in Piranha	15 min.
Rinse in DI	5-6 times
Soak in BHF	2-5 min.
Rinse in DI	5-6 times
Soak in SC1 (10 DI: 3 H_2O_2: 3 NH_4OH)	
on hotplate at 225°C	15 min.
Rinse in DI	5-6 times
Soak in BHF	2-5 min.
Rinse in DI	5-6 times
Soak in SC2 (10 DI: 3 H_2O_2: 3 HCL)	
on hotplate at 225°C	15 min.
Soak in BHF	2-5 min.
Rinse in DI	5-6 times
Soak in SC2 (10 DI: 3 H_2O_2: 3 HCL)	
on hotplate at 225°C	15 min.
Soak in BHF	2-5 min.
Rinse in DI	5-6 times

Blow dry with N_2 making sure before picking

up wafer with tweezers the corner is dry

12. MOS oxidation _____

Used Blue-M

batch 1:	1130°C 2.5 hrs in O_2 ambient
	0.5 hrs in Ar ambient
batch 2:	1130°C 3 hrs in O_2 ambient
	0.5 hrs in Ar ambient

13. Deposit Al contacts _____

Used NRC evaporator

evaporated ~ three 1cm Al bars

14. For Schottky devices Deposit Ni contacts _____

Used the Varian E-beam evaporator

Evaporated 500 Angstroms of Ni metal

15. Lithography _____

Hardbake sample	120°C 10 min.
Apply HDMS to sample	- 25 psi 2 min.
Spin on positive photoresist (AZ 1518)	5000 RPM 40 sec.
Softbake sample	85°C 15 min.
Cool sample	30 min.
Mount on SUSS MJB-3 mask aligner	
Align mask #1	
Expose	
Standard Hard Contact Mode	
UV light	23 mW 7.5 sec.
For Schottky devices	
Develop in 1 AZ developer: 5 DI	35 sec.
For MOS devices	
Develop in 1 AZ 351 developer: 1 DI	1 min.
Rinse in running DI	1 min.

Blow dry with N_2
Inspect under microscope

For Schottky devices go to step 17
For MOS devices follow steps 16 and then continue from step 18

16. Pattern aluminum _____

Use Al wet etch solution	
(1 DI: 4 H_3PO_4: 1 CH_3COOH: 4 HNO_3)	20 min.
Rinse in DI	6 times
Blow dry with N_2	
Inspect under microscope	

17. Pattern Ni _____

Use Ni etch solution (1 HNO_3: 4 DI)	2 min.
Rinse in DI	6 times
Blow dry with N_2	
Inspect under microscope	

18. Strip positive photoresist (see step 6) _____

19. Solvent Clean (see step 7) _____

20. Fabout _____